

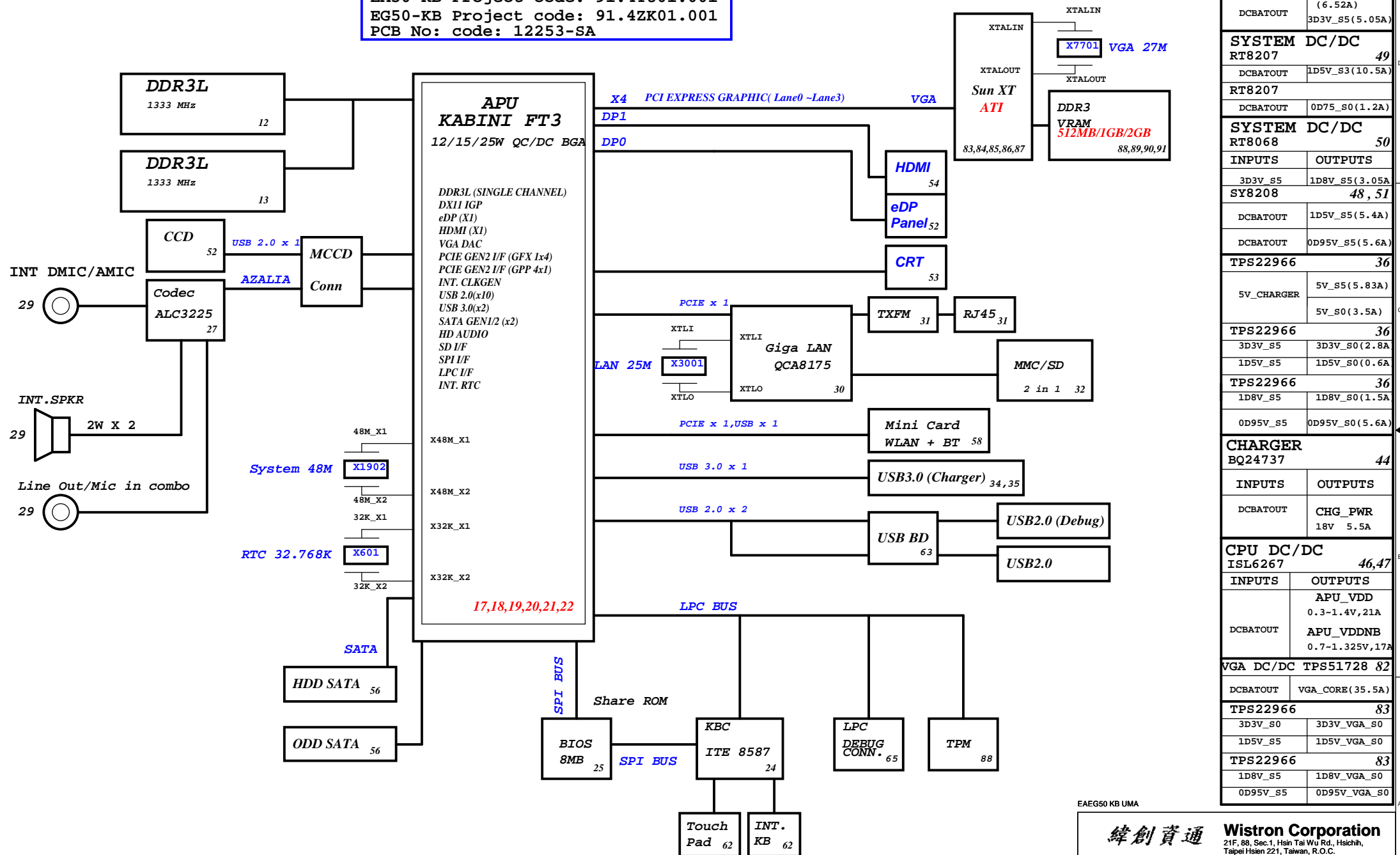
AMD KABINI EA/EG-40/50
PX /UMA Schematics Document
AMD FT3 APU
AMD GPU SUN XT M2/64bit

EAEG50 KB UMA

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Cover Page		
Size	Document Number	Rev
A4	KABINI	
Date: Wednesday, October 24, 2012		Sheet 1 of 102

AMD KABINI

EA40-KB Project code: 91.4ZF01.001
PCB No: code: 12247-SA
EA50-KB Project code: 91.4YU01.001
EG50-KB Project code: 91.4ZK01.001
PCB No: code: 12253-SA

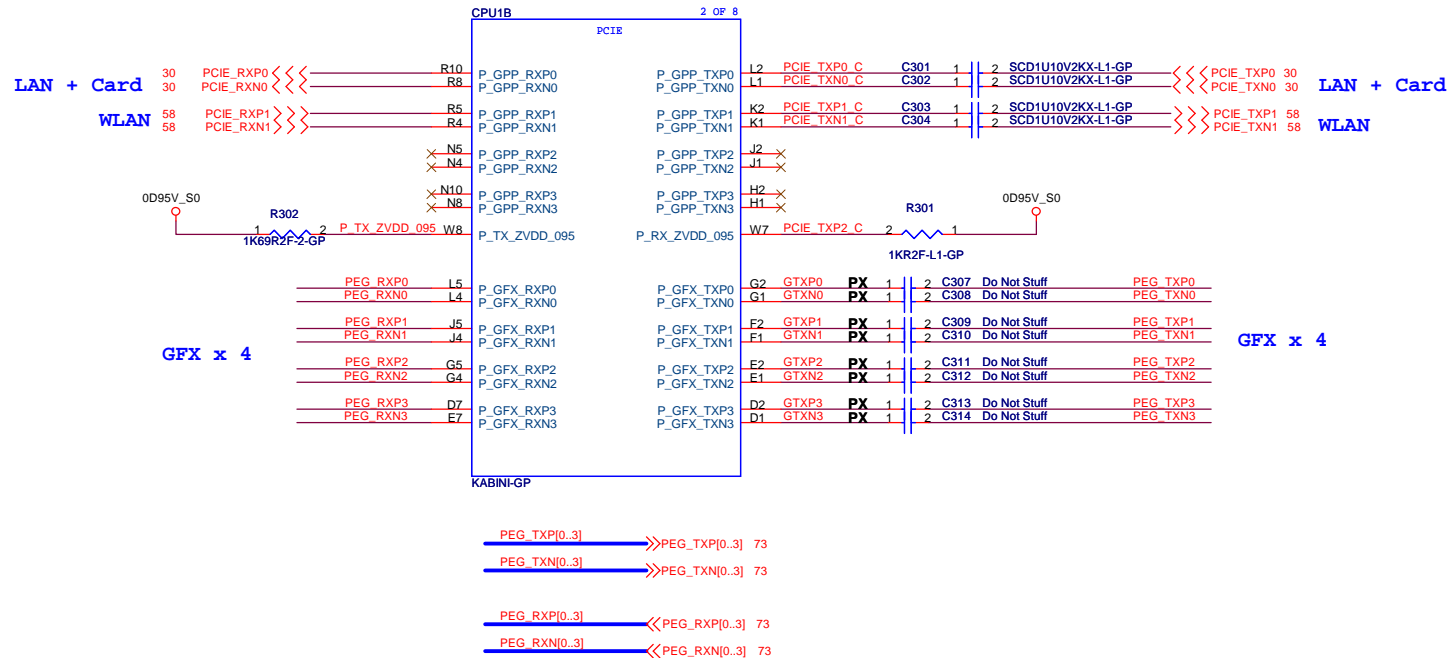


SYSTEM DC/DC		TPS51225	45
INPUTS	OUTPUTS		
DCBATOUT	5V_CHARGER (6.52A)	3D3V_S5	3D3V_S5(5.05A)
SYSTEM DC/DC		RT8207	49
DCBATOUT	1D5V_S3(10.5A)	RT8207	
DCBATOUT	0D75_S0(1.2A)		
SYSTEM DC/DC		RT8068	50
INPUTS	OUTPUTS		
3D3V_S5	1D8V_S5(3.05A)	SY8208	48, 51
DCBATOUT	1D5V_S5(5.4A)		
DCBATOUT	0D95V_S5(5.6A)		
TPS22966			36
5V_CHARGER	5V_S5(5.83A)		
	5V_S0(3.5A)		
TPS22966			36
3D3V_S5	3D3V_S0(2.8A)		
1D5V_S5	1D5V_S0(0.6A)		
TPS22966			36
1D8V_S5	1D8V_S0(1.5A)		
0D95V_S5	0D95V_S0(5.6A)		
CHARGER		BQ24737	44
INPUTS	OUTPUTS		
DCBATOUT	CHG_PWR	18V 5.5A	
CPU DC/DC		ISL6267	46,47
INPUTS	OUTPUTS		
DCBATOUT	APU_VDD 0.3~1.4V, 21A		
	APU_VDDNB 0.7~1.325V, 17A		
VGA DC/DC		TPS51728	82
DCBATOUT	VGA_CORE (35.5A)		
TPS22966			83
3D3V_S0	3D3V_VGA_S0		
1D5V_S5	1D5V_VGA_S0		
TPS22966			83
1D8V_S5	1D8V_VGA_S0		
0D95V_S5	0D95V_VGA_S0		

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Block Diagram			Rev
Size A3	Document Number	KABINI	
Date: Friday, February 01, 2013	Sheet 2 of 102		

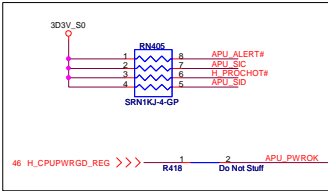


71.KABIN.B0U IC CPU Kabini 4110 1.5GHZ 15W4C FT3 ES2 BGA
71.KABIN.C0U IC CPU Kabini 5110 2.0GHZ 25W4C FT3 ES2 BGA

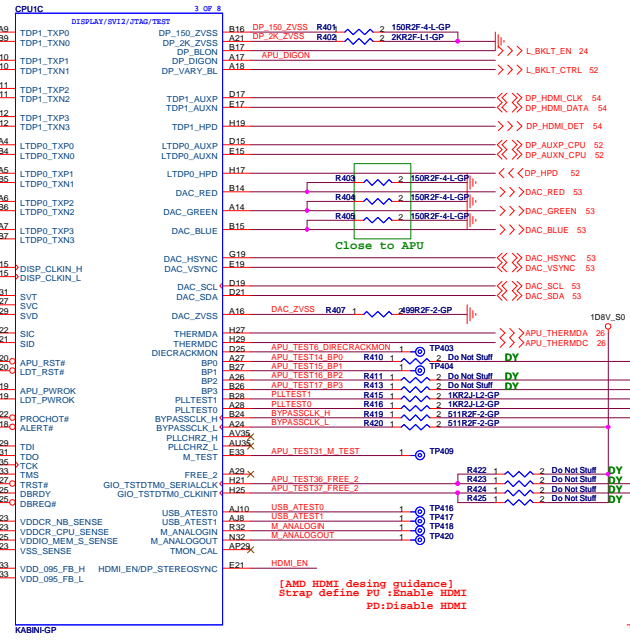
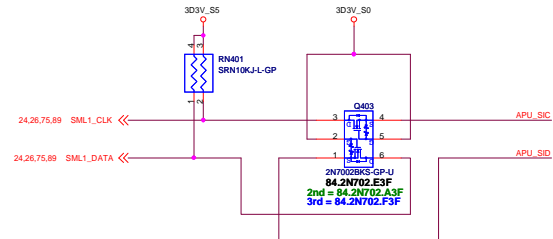
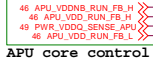
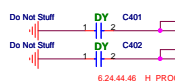
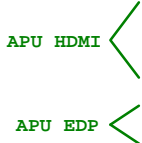
EAEG50 KB UMA



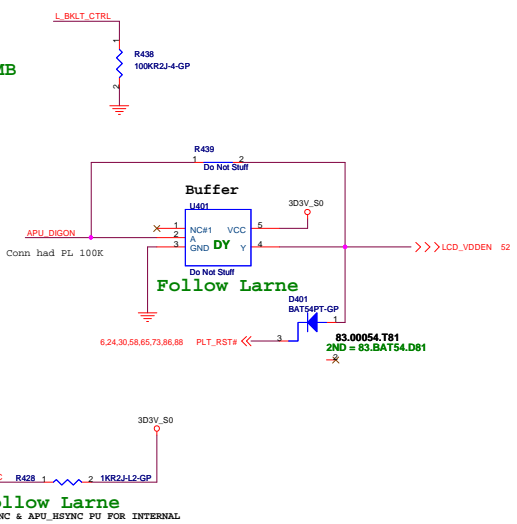
SVC	SVD	OUTPUT VOLTAGE (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

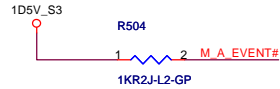


20120820 Follow Larne

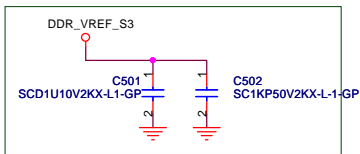


- APU EDP
- APU HDMI SMB
- APU EDP
- APU CRT

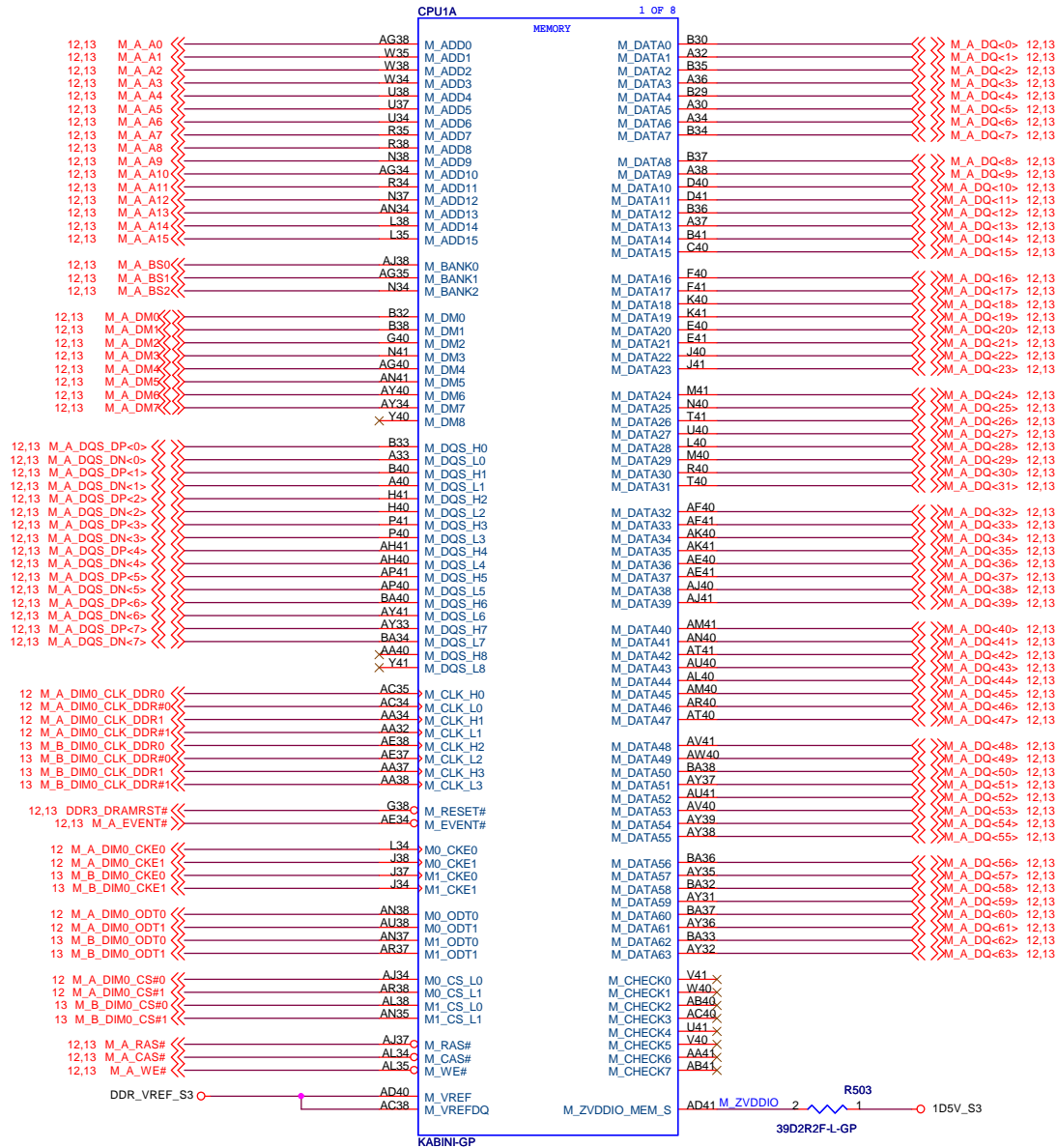




APU_VREF_DQ



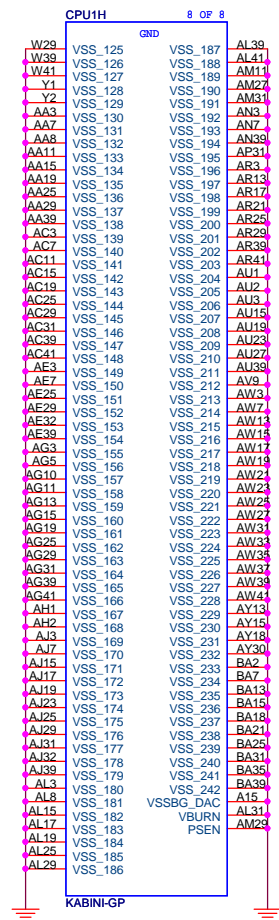
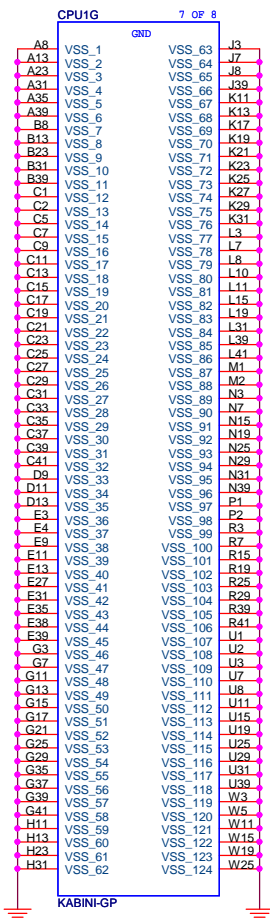
LAYOUT: place them close to APU



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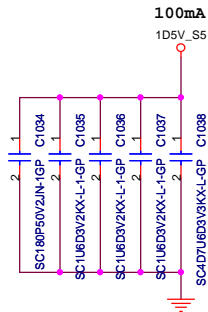
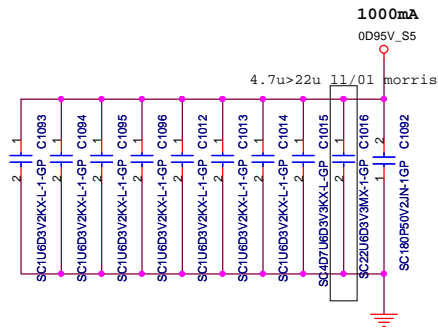
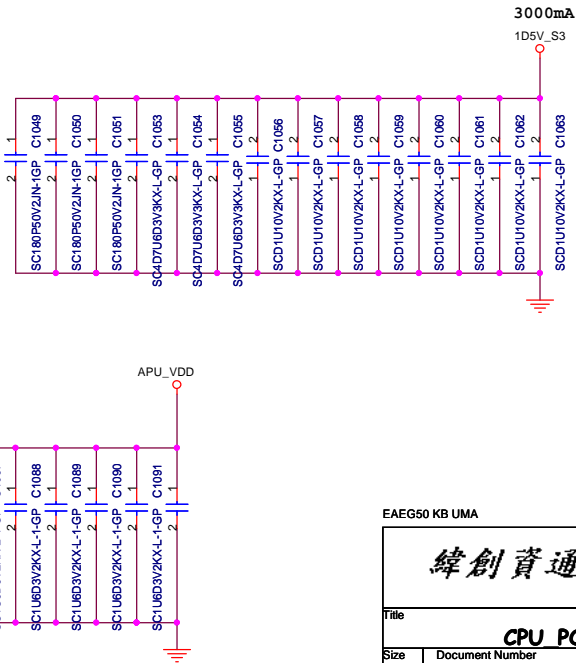
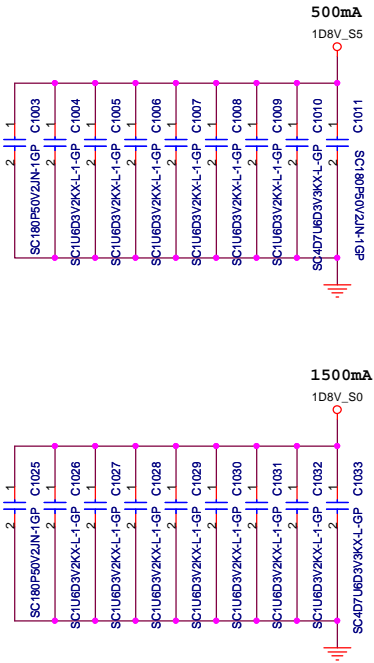
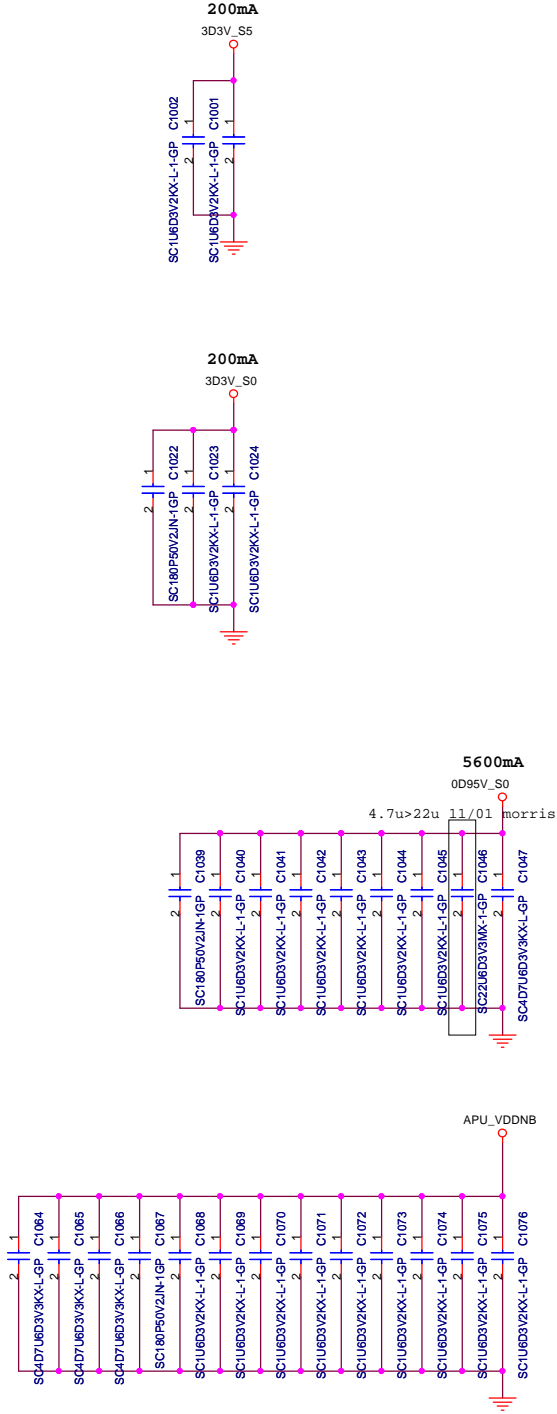
Title		
CPU DDR		
Size	Document Number	Rev
A3	KABINI	
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Title		
CPU VSS		
Size	Document Number	Rev
A3	KABINI	
Date:	Wednesday, November 28, 2012	Sheet 9 of 102



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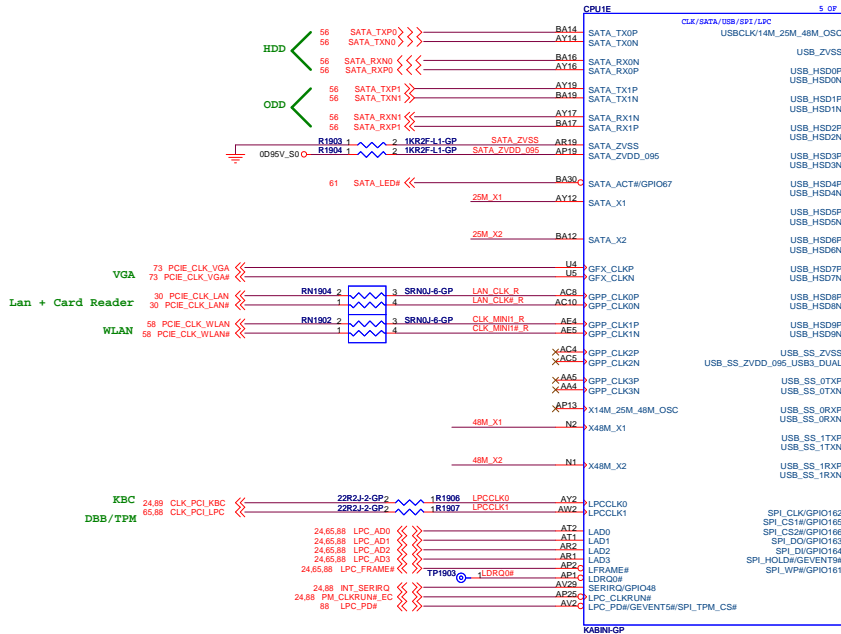
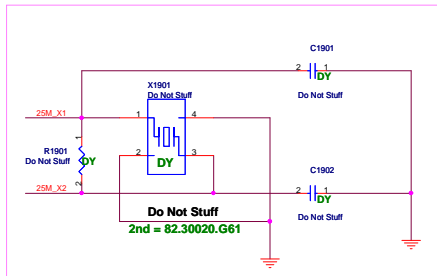
Title		
CPU POWER CAP1		
Size	Document Number	Rev
A3	KABINI	
Date:	Tuesday, January 15, 2013	Sheet 10 of 102

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SATA Table

0	HDD
1	ODD

SB 11/27 25M XTAL Reserved for AMD

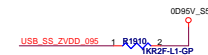


USB Table

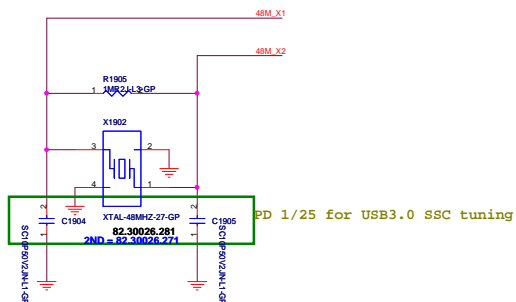
Pair	Device
0	USB2.0 Debug (DB Conn)
1	USB2.0 (DB Conn)
2	Touch Panel
3	
4	CCD (CCD Conn)
5	WLAN + BT (Mini PCI-E)
6	
7	
0/8	USB3.0 & USB 2.0 Charger (MB)
1/9	

Xtal Table

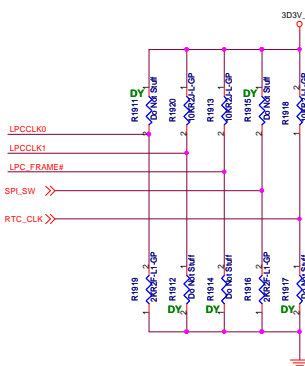
	System & USB	CLK
0	RTC	48M
1	SATA	32.768K
2	LAN	25M
3	VGA	25M
4		27M



SPI SHARE ROM



SYSTEM STRAPPINGS



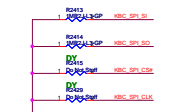
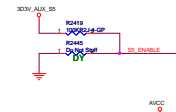
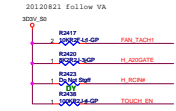
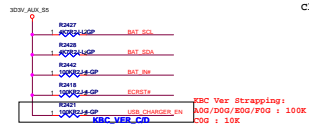
	LPC_CLK0	LPC_CLK1	LFRAME#	EXPCARD_PCIE_PWREN#	RTC_CLK
FULL	BOOT FAIL TIMER ENABLED	CLNGEN ENABLED	SPI ROM	1.0V SPI ROM (DEFAULT)	NORMAL POWR UP/RESET TIMING (DEFAULT)
HIGH		DEFAULT	DEFAULT		
FULL	BOOT FAIL TIMER DISABLED	CLNGEN DISABLED	LPC ROM	3.0V SPI ROM	FAST POWER UP/RESET TIMING FOR SIMULATION
LOW	DEFAULT				

EAE650 KB UMA

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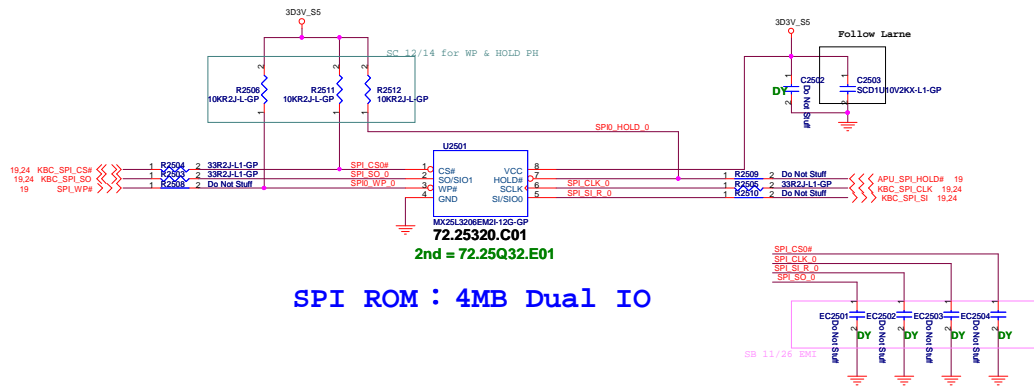
Title	Document Number	Rev
CPU SATA/USB/LPC/SPI/CLK	KABINI	
Date: Monday, February 04, 2013	Sheet 19 of 102	

SSID = KBC



SSID = Flash.ROM SPI FLASH ROM (4M byte) for KBC

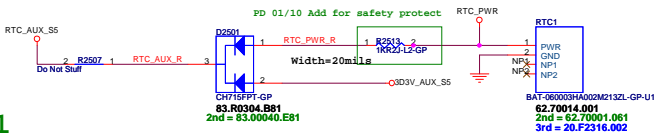
PD 1/28 SPI ROM : 4MB Dual IO
1st. MXIC : 72.25320.C01
2nd. WINBOND : 72.25Q32.E01
(手置件)請PCC移至DIP件



SPI ROM : 4MB Dual IO

SSID = RBAT

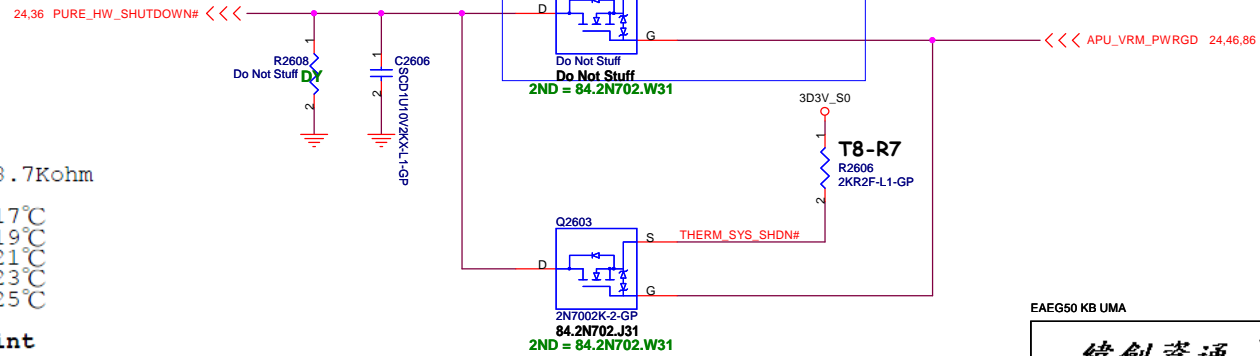
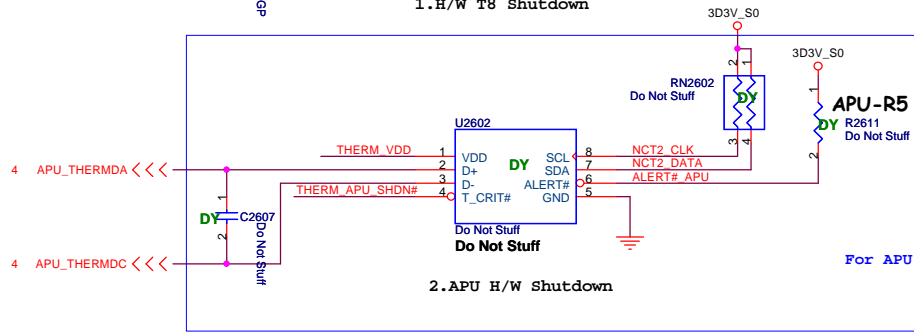
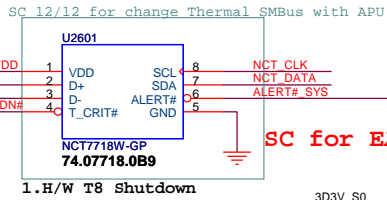
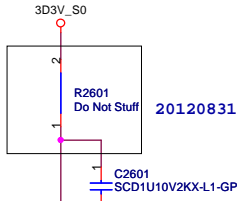
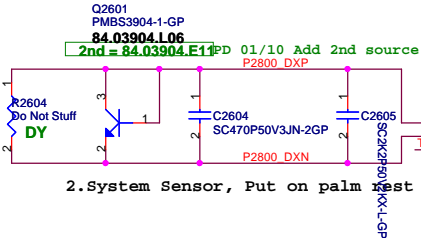
CR2032額外備料:
1.KTS: 23.20068.001
2.DBV: 23.22065.001



SSID = Thermal

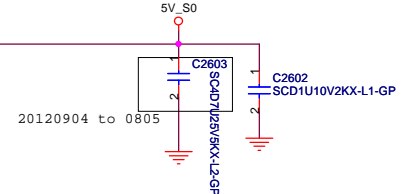
Thermal sensor NCT 7718W

Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.



SC EA50 DY RN2604 , mount RN2603

24,86 FAN1_PWM >>>
86 FAN_TACH1_C >>>
For AFTE



ALERT# /T CRIT#
Pull-up Resistor

R5	R7				
	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77°C	87°C	97°C	107°C	117°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	83°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C

T_CRIT temperature strapping point

T8=85 degree
SYS=85 degree
APU=125 degree

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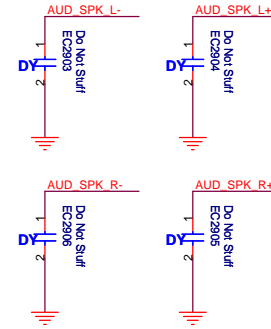
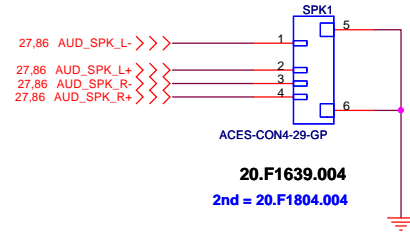
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Title Thermal 7718/Fan Controller P2793		
Size	Project Name KABINI	Rev SA
Date: Monday, February 04, 2013	Sheet 26	of 102

SSID = AUDIO

Speaker

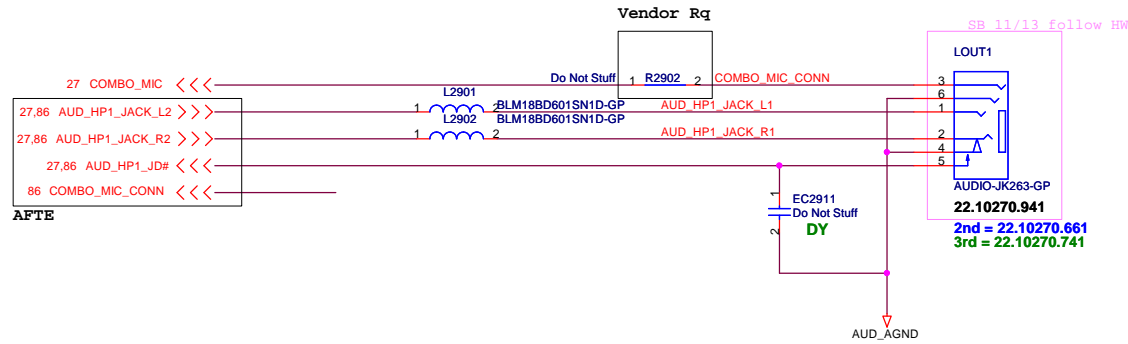
2W 4ohm X 2 speaker



Layout Note:

Trace width=40mil

Combo Jack



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Title		Audio Jack	
Size	Project Name	KABINI	
Date: Monday, February 04, 2013	Sheet	29	of 102
Rev		SA	

Power-On-Strapping Table

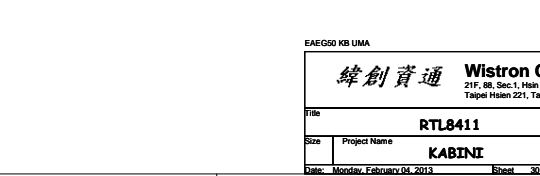
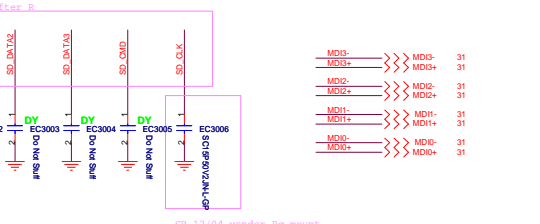
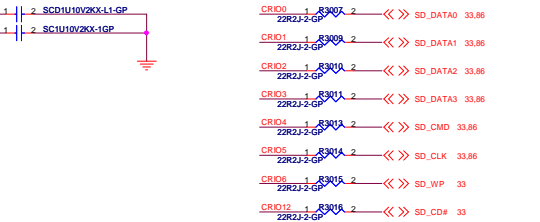
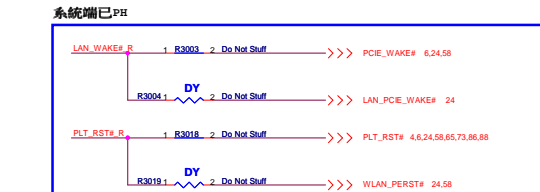
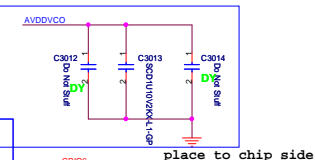
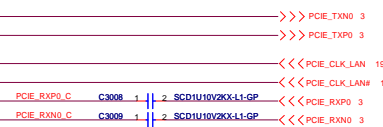
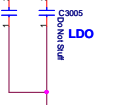
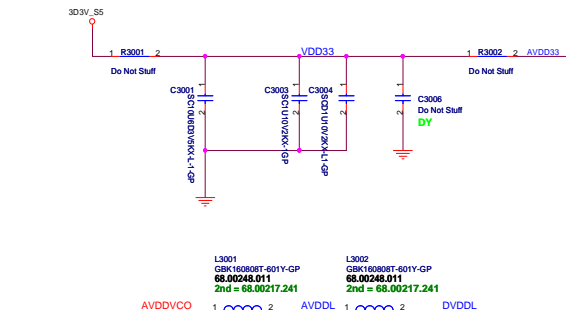
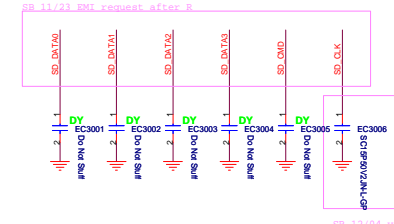
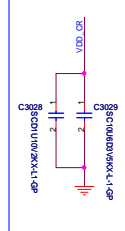
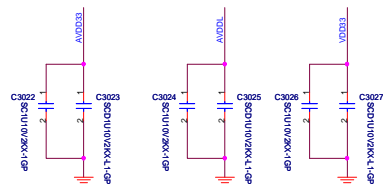
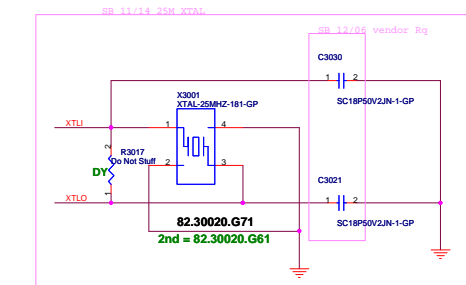
Pin	Description
LED[1]	1 Switch mode regulator (SWR) select 0 Linear regulator (LDO) select
LED[3]	1 25MHz clock input 0 48MHz clock input
[CRIO14, CRIO7]	10 1. Support xD, not support SPI. 2. Can support PPS, PPS at LED[0] or LED[1] or LED[2] which is selected by eFuse. 01 1. Support SPI, not support xD. 2. Can support PPS, PPS at LED[0] or LED[1] or LED[2] which is selected by eFuse. 11 1. Not support xD, not support SPI. 2. Only Support PPS, PPS always at CRIO13.

PPS is used for IEEE 1588 timing synchronization and is an output pin to output an accurate 1Hz clock. Currently this pin can be floating.

Check!!

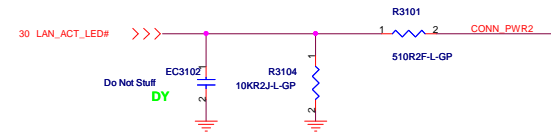
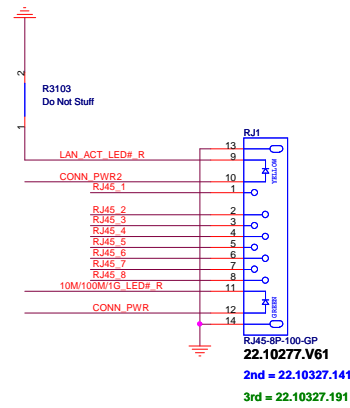
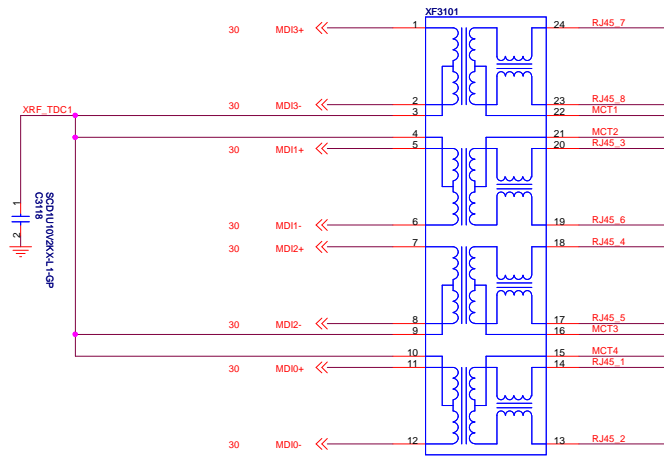
ISOLATn is active low to isolate the whole chip to place in lowest power consumption mode.

place at chip side FAE suggest

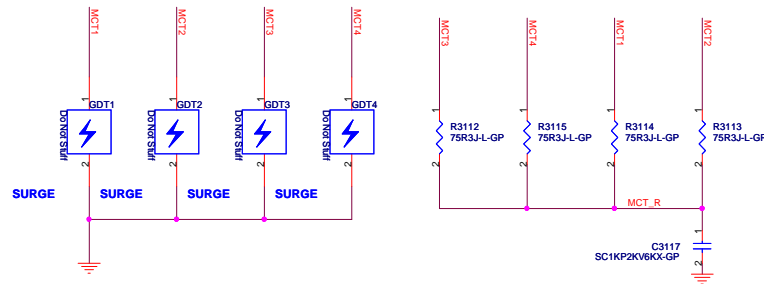
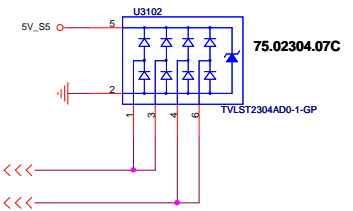
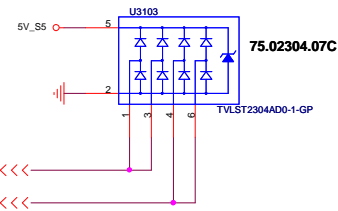
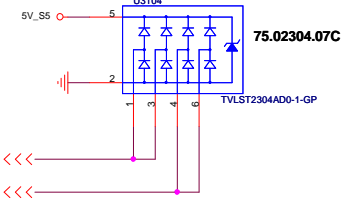
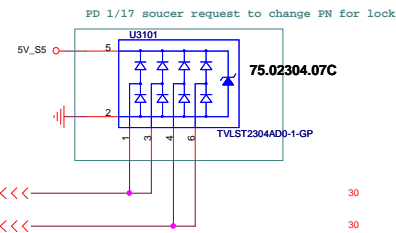
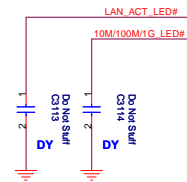
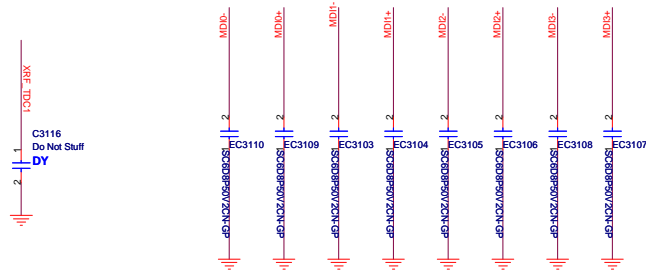
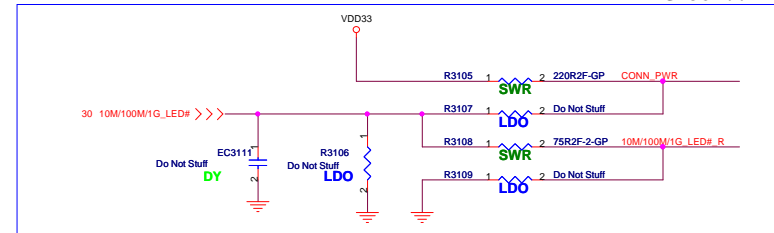


CRIQ[0:14]	CRIQ[0:14]	xD_CEn	xD_CEn
CRIQ14	CRIQ14	xD_ALE	xD_ALE
CRIQ13	CRIQ13	xD_RDBYn	xD_RDBYn
CRIQ12	CRIQ12	xD_RDBYn	xD_RDBYn
CRIQ11	CRIQ11	xD_RDBYn	xD_RDBYn
CRIQ10	CRIQ10	xD_RDBYn	xD_RDBYn
CRIQ09	CRIQ09	xD_RDBYn	xD_RDBYn
CRIQ08	CRIQ08	xD_RDBYn	xD_RDBYn
CRIQ07	CRIQ07	xD_RDBYn	xD_RDBYn
CRIQ06	CRIQ06	xD_RDBYn	xD_RDBYn
CRIQ05	CRIQ05	xD_RDBYn	xD_RDBYn
CRIQ04	CRIQ04	xD_RDBYn	xD_RDBYn
CRIQ03	CRIQ03	xD_RDBYn	xD_RDBYn
CRIQ02	CRIQ02	xD_RDBYn	xD_RDBYn
CRIQ01	CRIQ01	xD_RDBYn	xD_RDBYn
CRIQ00	CRIQ00	xD_RDBYn	xD_RDBYn

SSID = LAN



Check!!



```

86 RJ45_1 >>>_____
86 RJ45_2 >>>_____
86 RJ45_3 >>>_____
86 RJ45_4 >>>_____
86 RJ45_5 >>>_____
86 RJ45_6 >>>_____
86 RJ45_7 >>>_____
86 RJ45_8 >>>_____

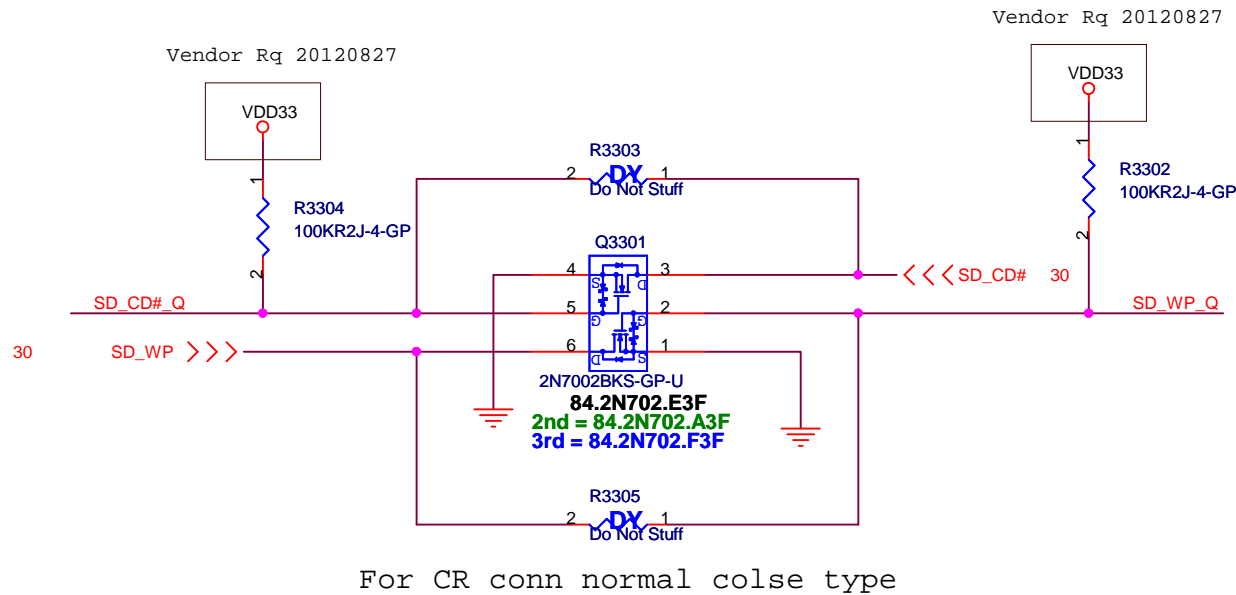
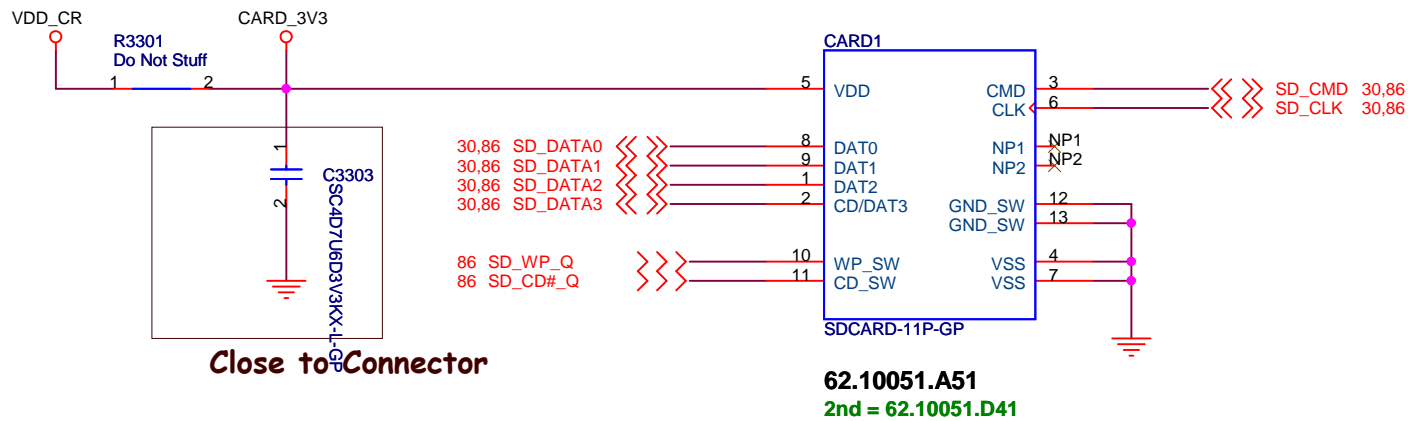
86 LAN_ACT_LED#R >>>_____
86 10M/100M1G_LED#R >>>_____
86 CONN_PWR >>>_____
86 CONN_PWR2 >>>_____

```

For AFTE

SSID = SDIO

SD//MS Card Reader



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緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CARD Reader CONN

Size

Project Name

KABINI

Rev

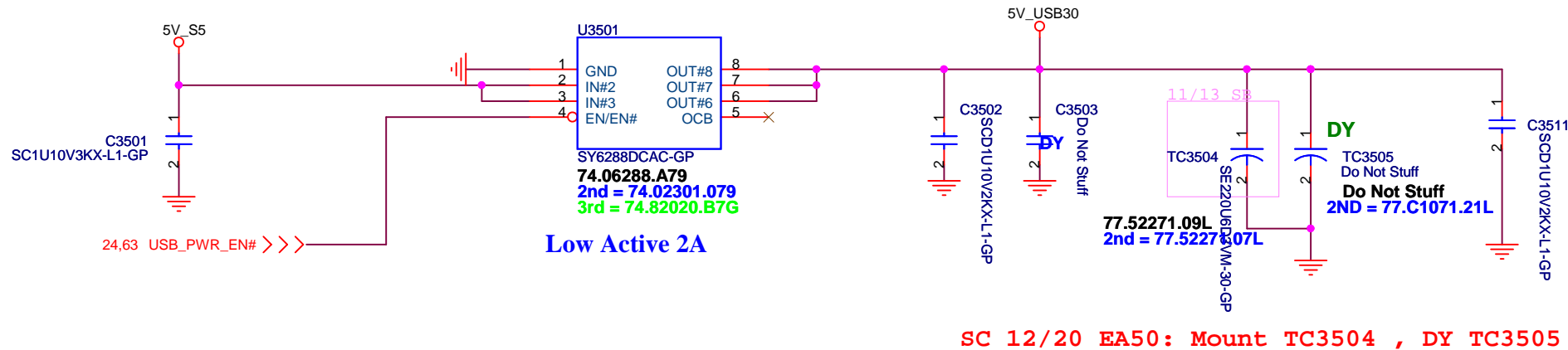
SA

Date: Monday, February 04, 2013

Sheet 33 of 102

2

1



EAEG50 KB UMA

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB_Charger

Size

Project Name

KABINI

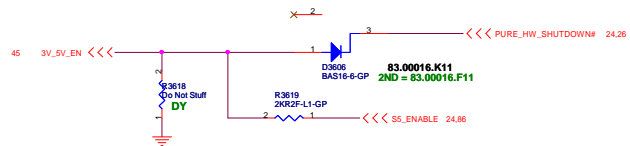
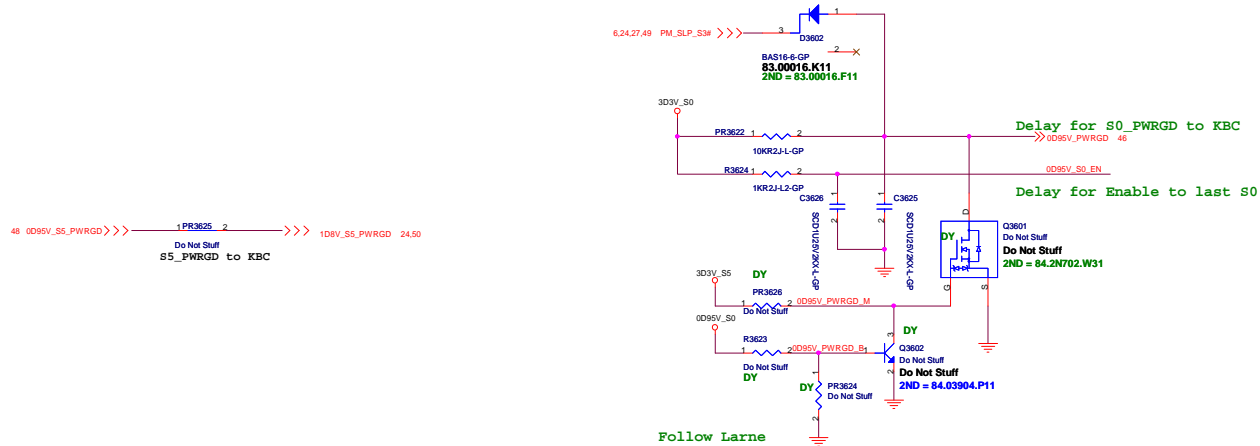
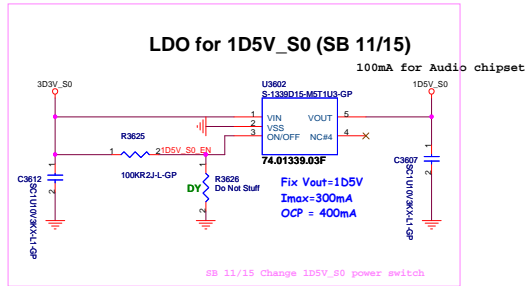
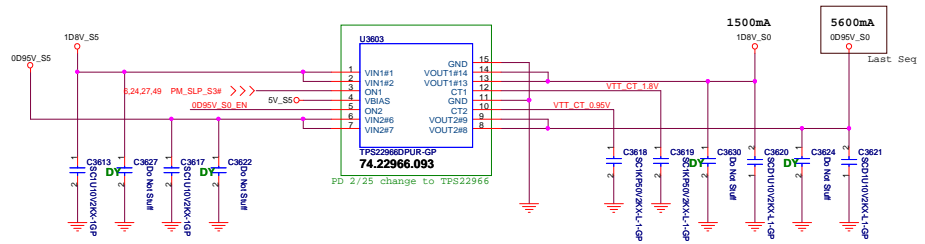
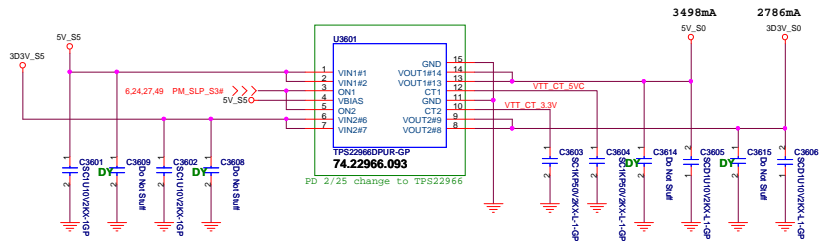
Rev

SA

Date: Monday, February 04, 2013

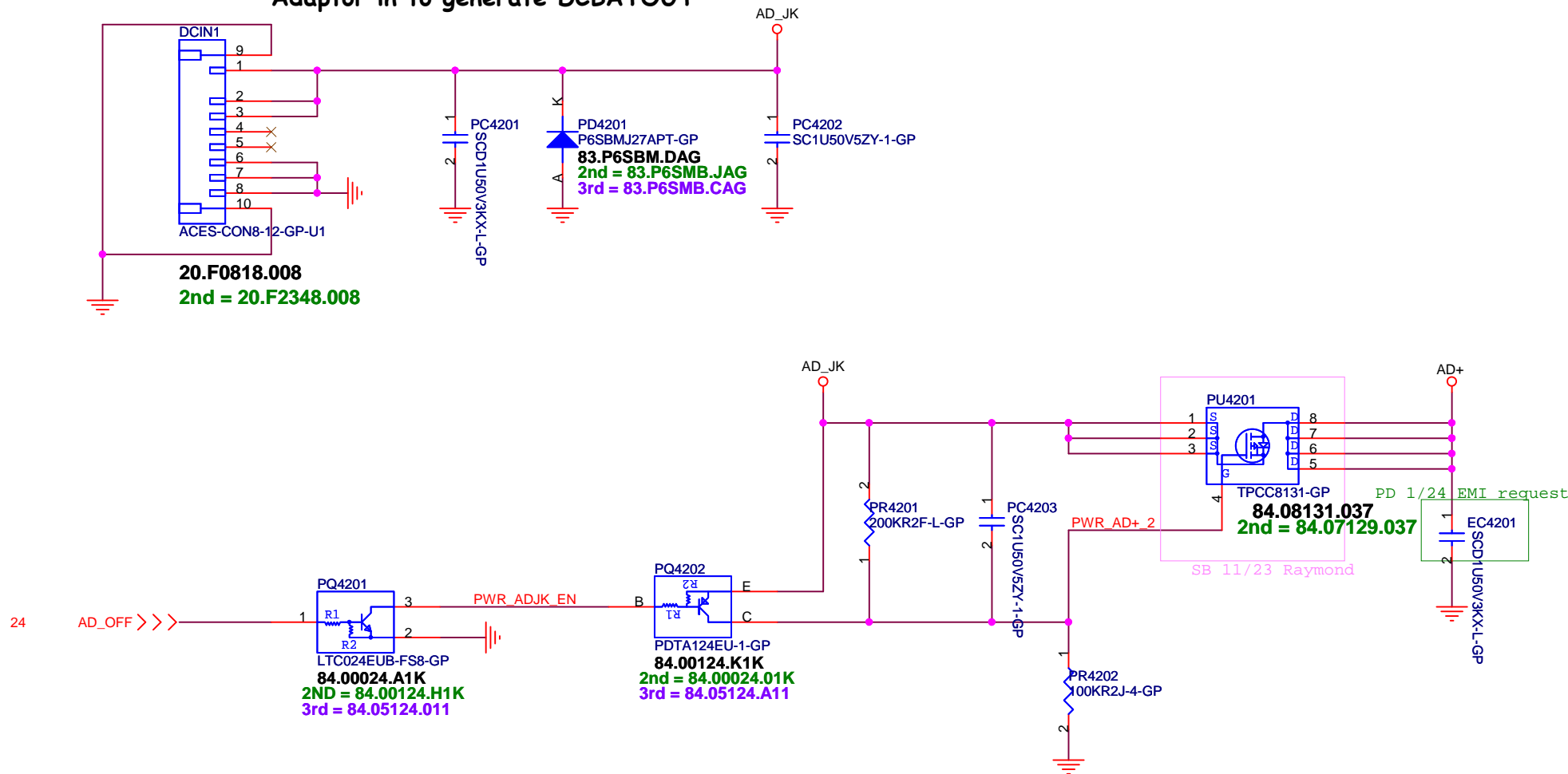
Sheet 35 of 102

Power Sequence



ANNIE solution

Adaptor in to generate DCBATOUT



EAEG50 KB UMA

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

DCIN JACK

Size

Project Name

KABINI

Rev

SA

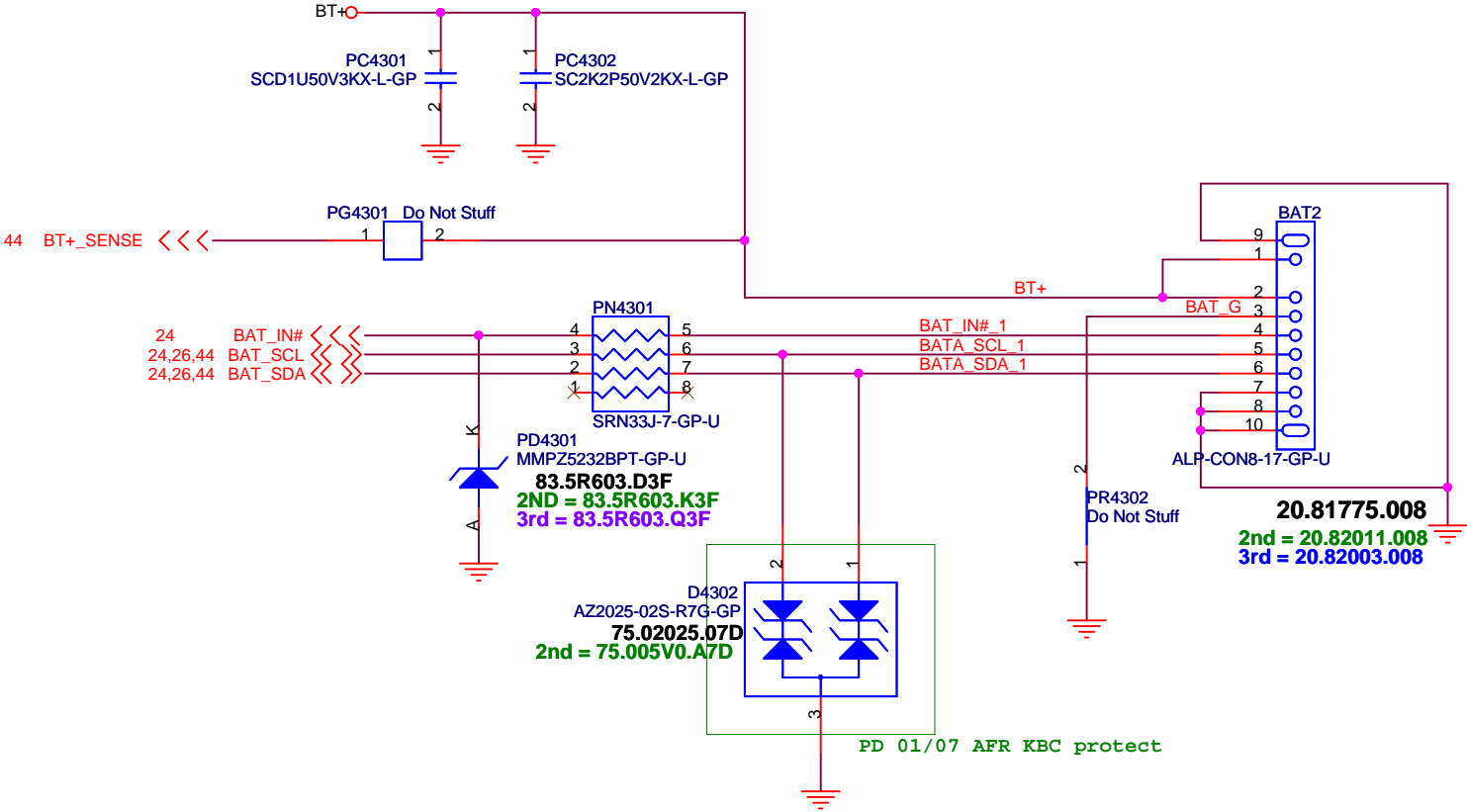
Date: Tuesday, February 19, 2013

Sheet 42 of 102

BATTERY CONNECTOR

86	BATA_SDA_1	>>>	_____
86	BATA_SCL_1	>>>	_____
86	BAT_IN#_1	>>>	_____
86	BAT_G	>>>	_____

For AFTE



EAEG50 KB UMA

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
BATT CONN			
Size	Project Name		Rev
	KABINI		SA
Date: Wednesday, February 20, 2013		Sheet 43	of 102

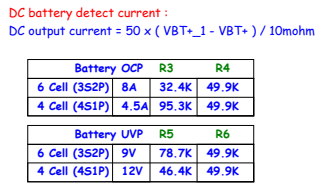
SSID = Charger

AD+

PR4407, PR4401

AD+ total power	R1	R2
65w 105%	18.7K	100K
90w	65k	100K

Change the table to stop charge%



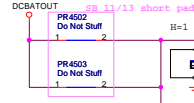
SSID = PWR.Plane.Regulator_3p3v5v

Cut off itself

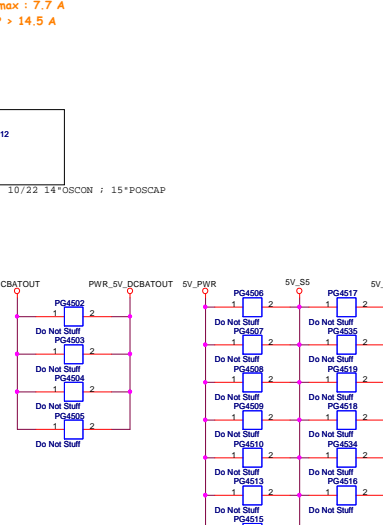
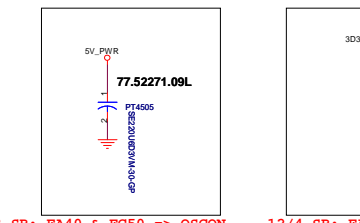
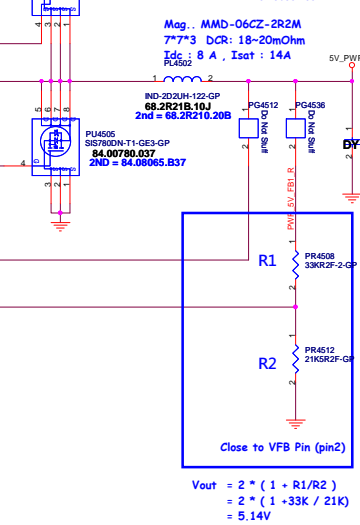
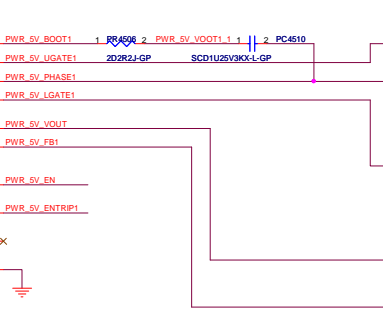
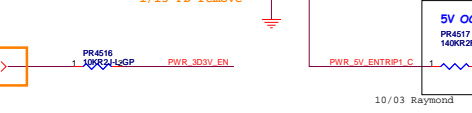
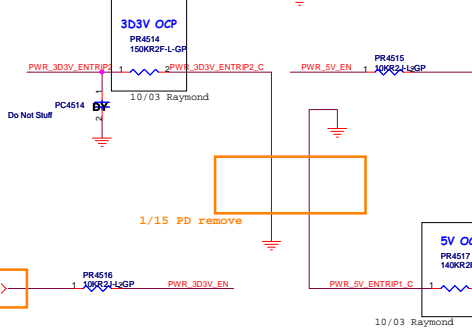
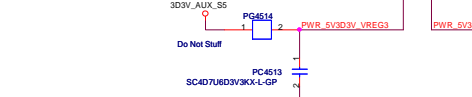
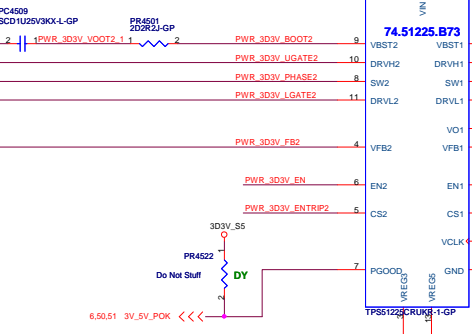
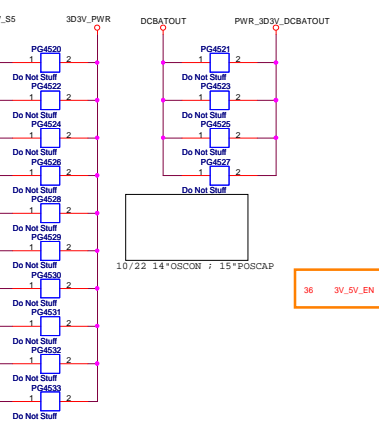
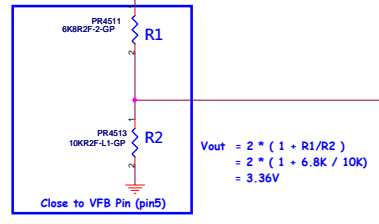
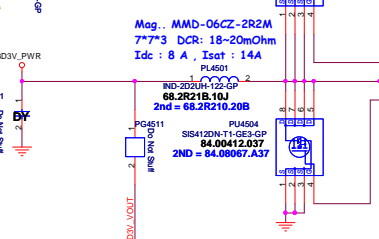
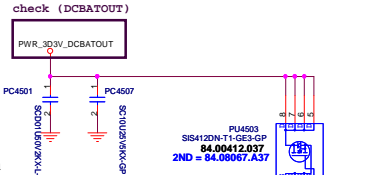
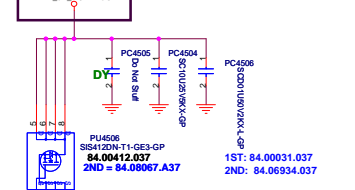
check (UVP)

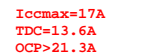
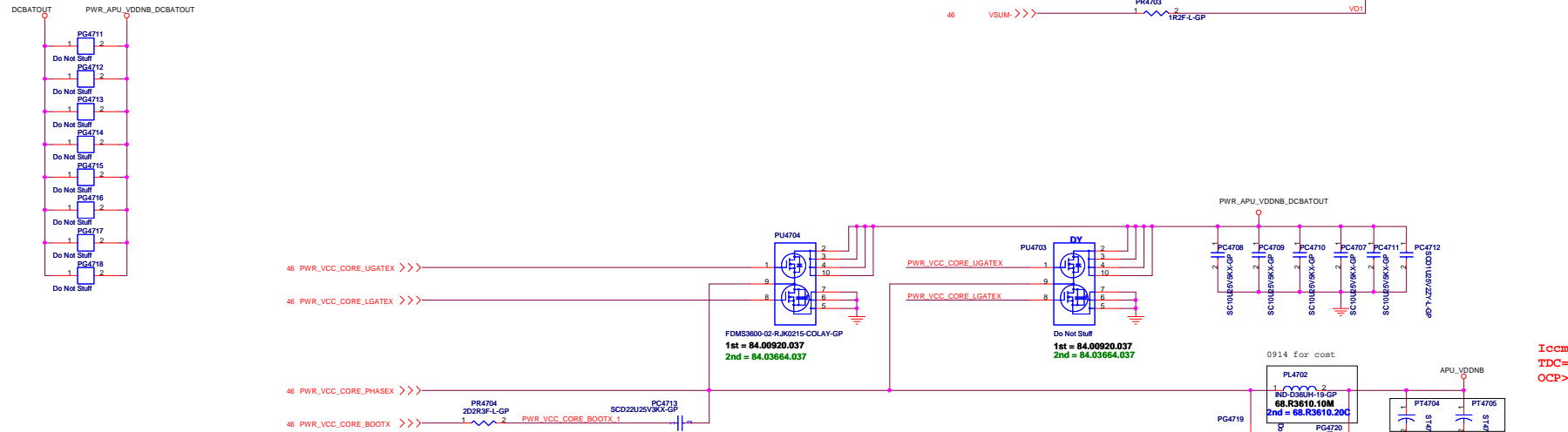
check (DCBATOUT)

check (DCBATOUT)



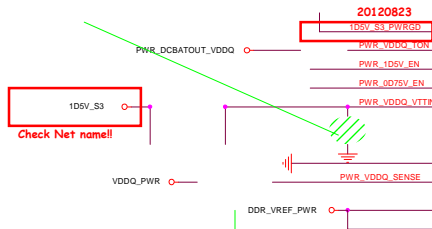
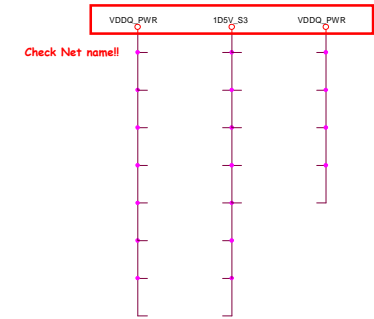
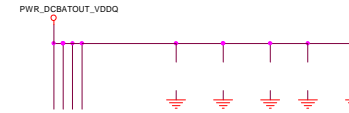
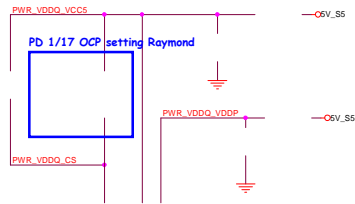
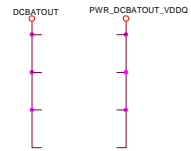
check (DCBATOUT)



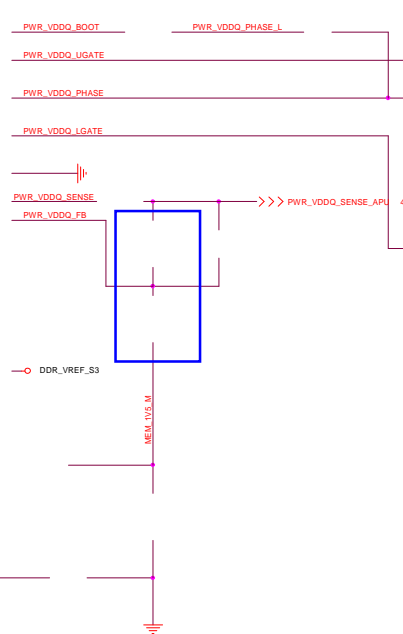
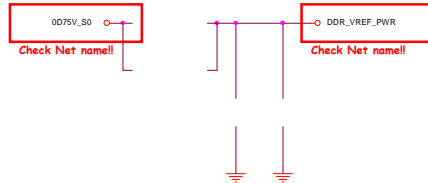


WWW.AliSaler.Com

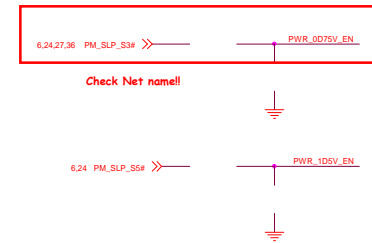
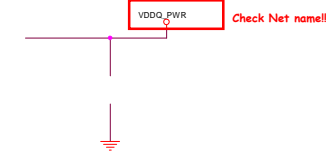




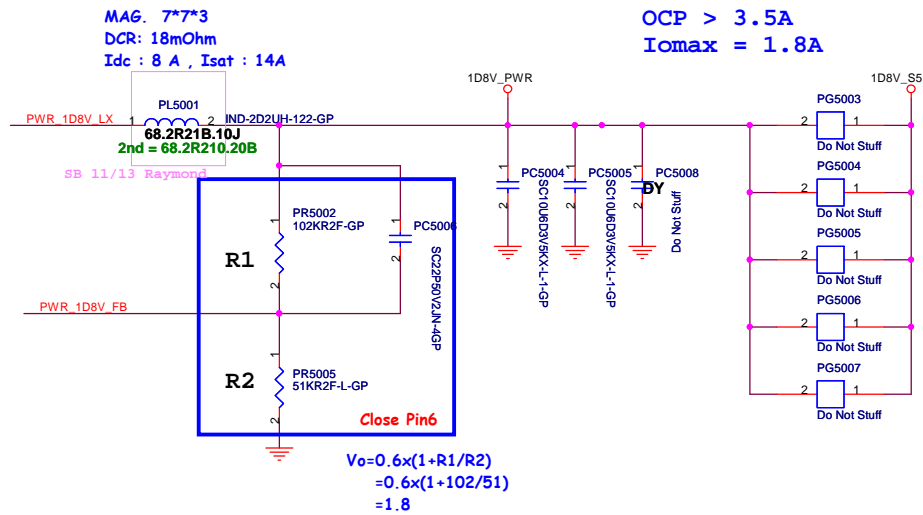
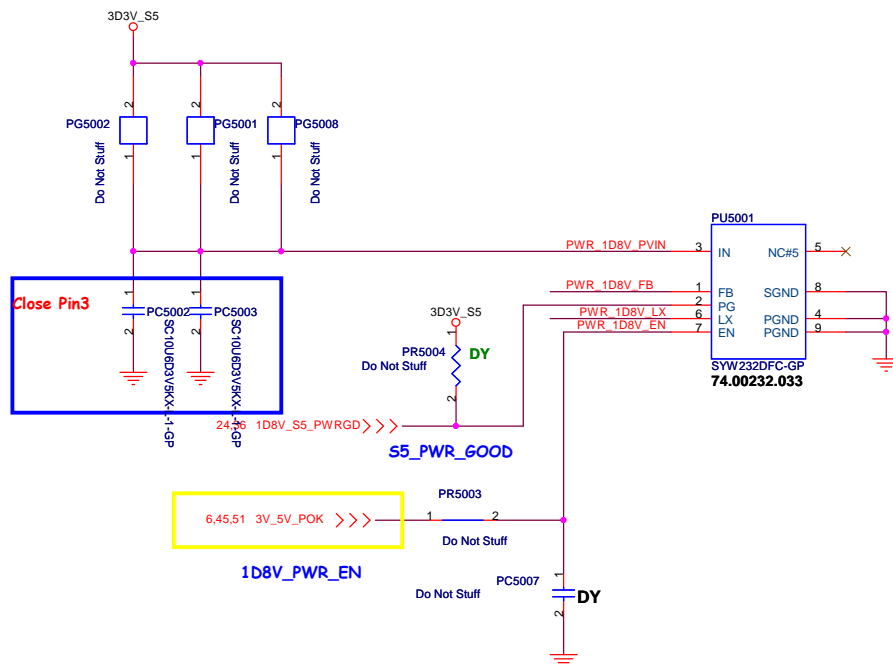
Iomax=1A
OCP>1.5A
Close to output cap pin1, not
inside of the output cap



CYNTec. 0.68uH 7*7*3
DCR= 5 ~ 5.5 mohm
Idc=15.5A, Isat=25A



SSID = PWR.Plane.Regulator_1p8v



EAEG50 KB UMA

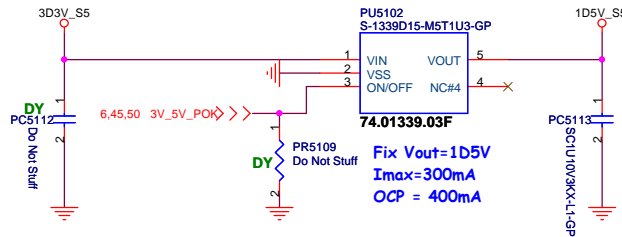
緯創資通 Wistron Corporation

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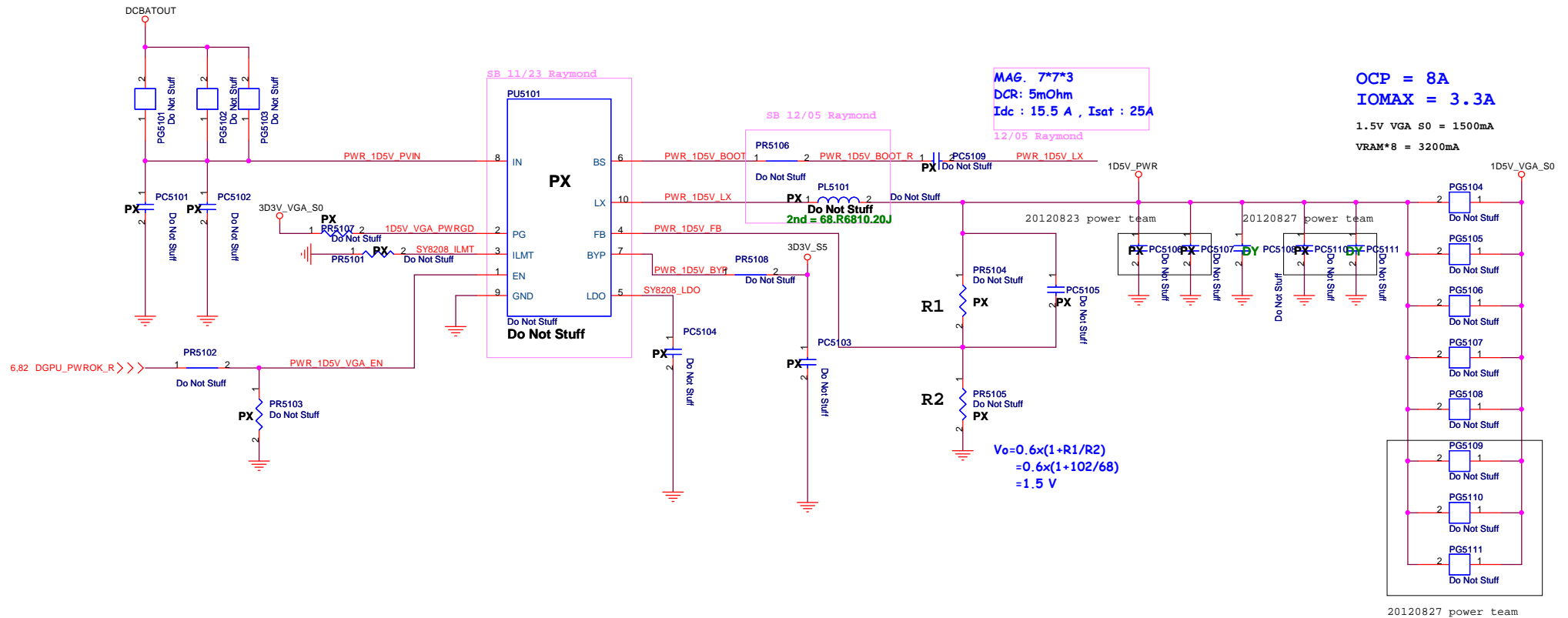
Title			1D8V_S0 SYW232
Size	Document Number	KABINI	
A3			
Date:	Monday, February 04, 2013	Sheet	50 of 102

LDO for 1D5V_S5 (SB 11/13)

1.5V S0 = 100mA(VDDIO_AZ) + 100mA(Audio) + 600mA(Minicard DY) = 200mA



SY8208D for 1D5V_VGA_S0 (SB 11/13)



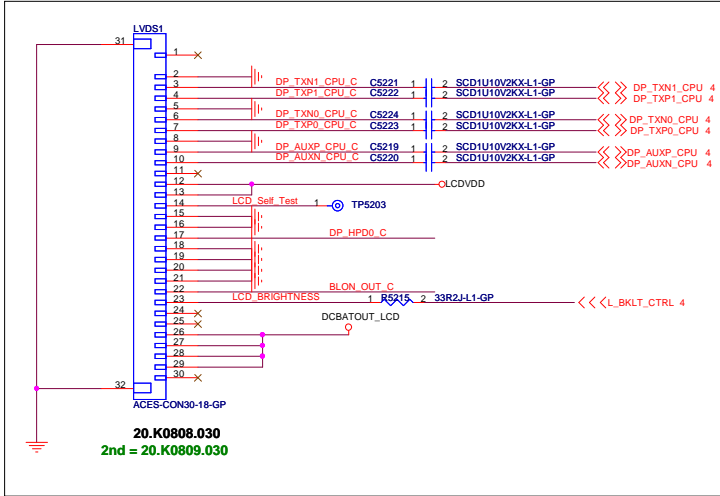
EAEG50 KB UMA

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Title			1D5V_S5 SY8208D
Size	Document Number	KABINI	
A3			
Date:	Tuesday, February 19, 2013	Sheet	51 of 102

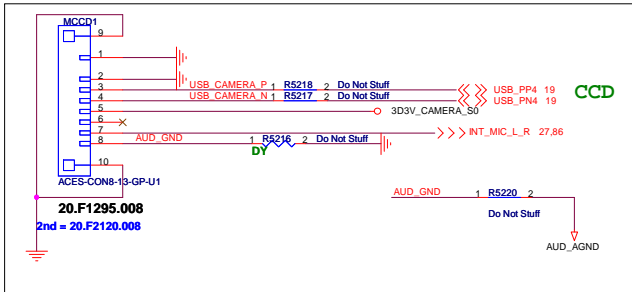
SSID = VIDEO

eDP Conn.



10/04 change to 20.K0808.030 for ME request

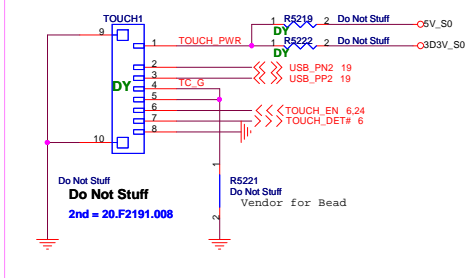
Camera+MIC Conn.



10/03 change to 8pin for del DMIC

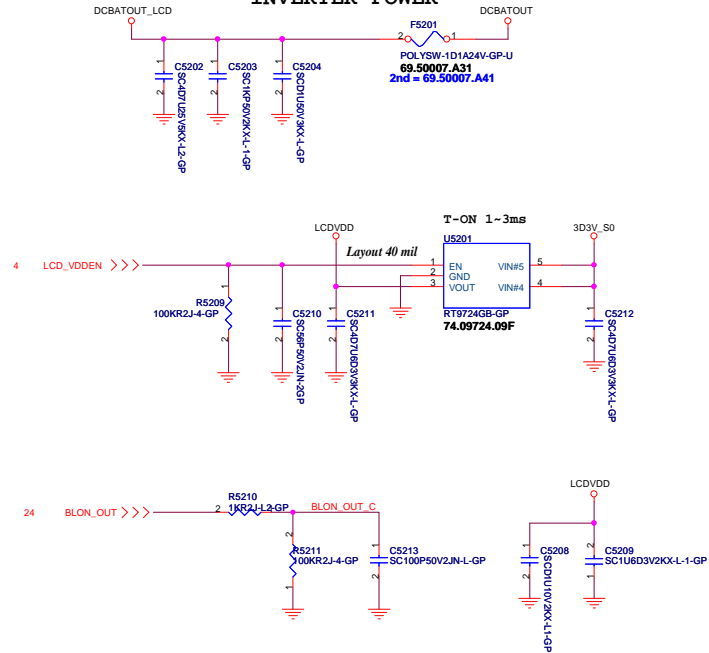
10/15 change to 20.F1295.008 follow HW

Touch Conn.

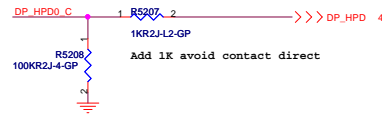


SC NO support

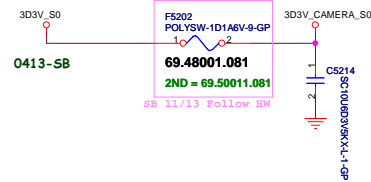
INVERTER POWER



EDP HPD High active



Camera Power

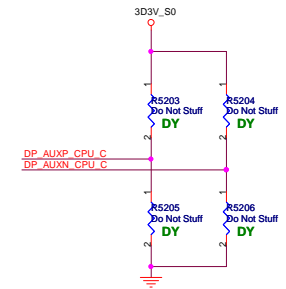


```

86 AUD_GND <<< _____
86 DP_HP00_C >>> _____
86 BLON_OUT_C >>> _____
86 LCD_BRIGHTNESS >>> _____
86 DP_TXN1_CPU_C >>> _____
86 DP_TXP1_CPU_C >>> _____
86 DP_TXN0_CPU_C >>> _____
86 DP_TXP0_CPU_C >>> _____
86 DP_AUXP_CPU_C <<< _____
86 DP_AUXN_CPU_C <<< _____

```

For AFTE



EAEG50 KB UMA

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Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

LCD Connector

Size

Project Name	
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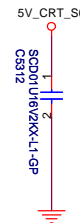
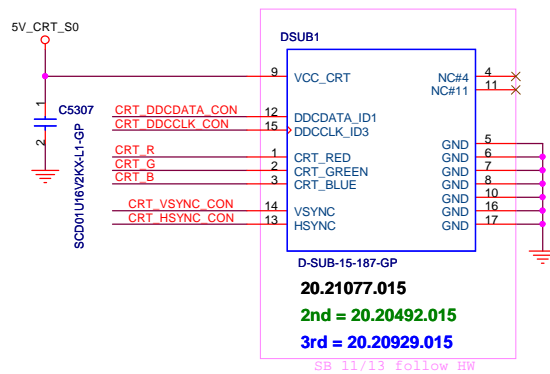
KABINI

Date: Monday, February 25, 2013

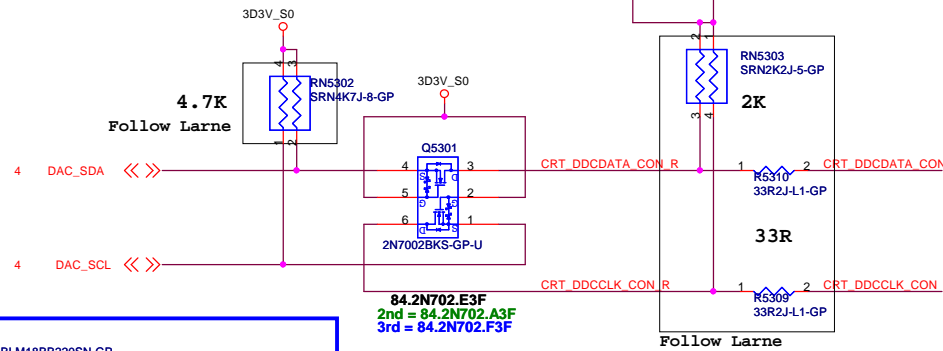
Sheet	52
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Rev

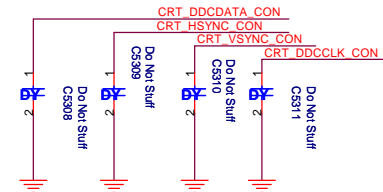
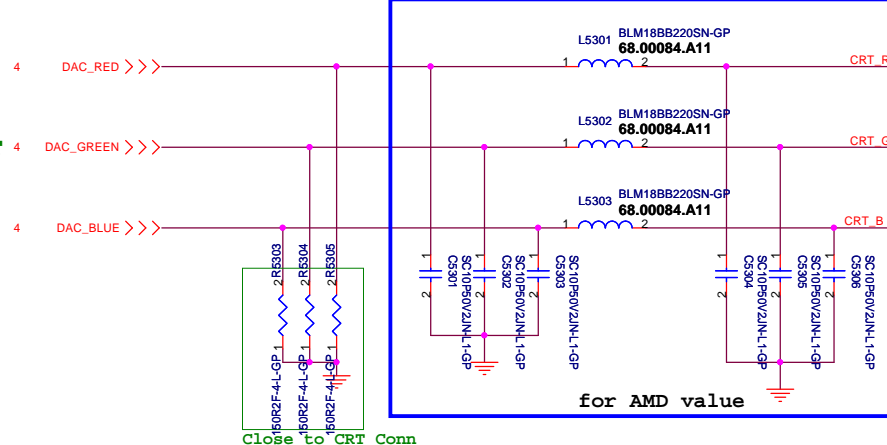
2	SA
---	----



CRT DDCDATA & DDCCLK level shift

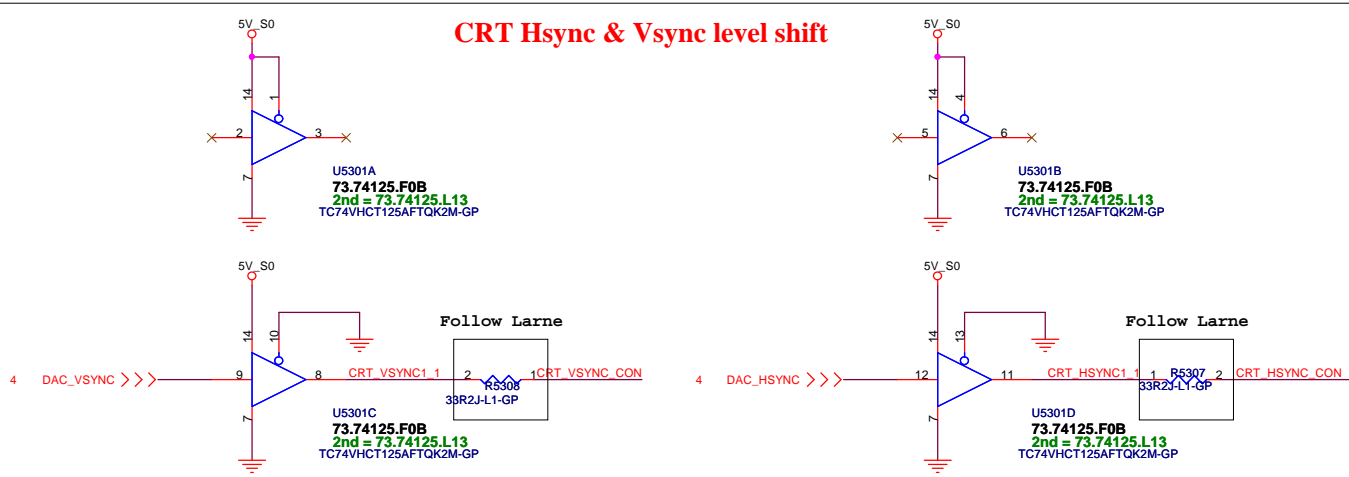


APU to CRT



10/16 follow COMAL

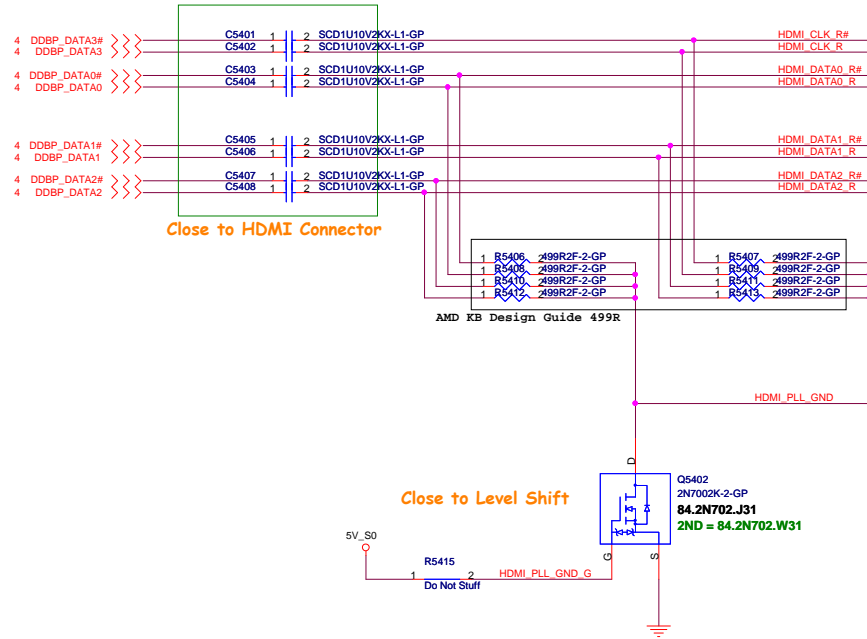
CRT Hsync & Vsync level shift



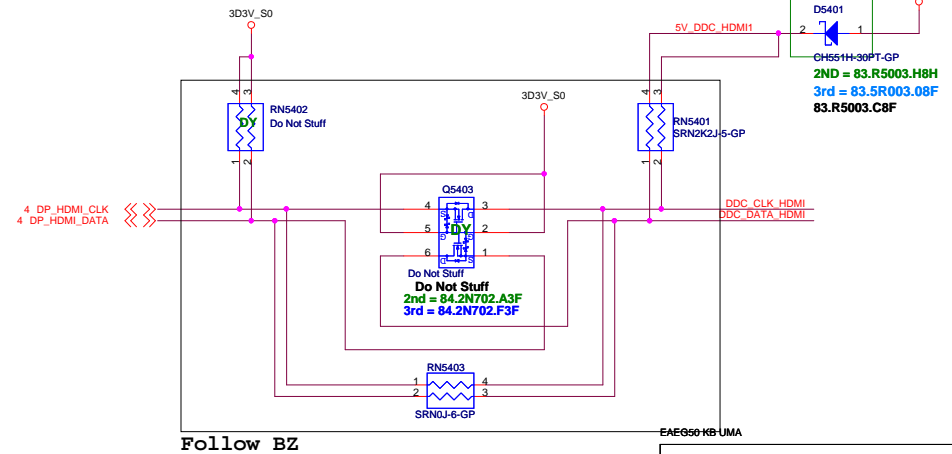
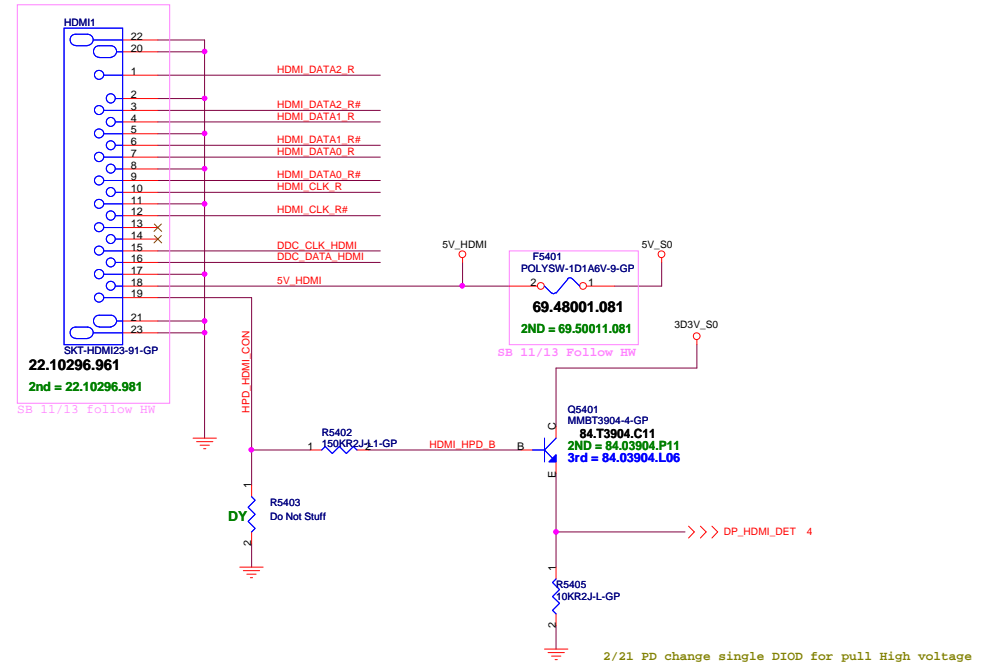
EAEG50 KB UMA

SSID = VIDEO

HDMI Level Shifter & CONNECTOR



HDMI CONN

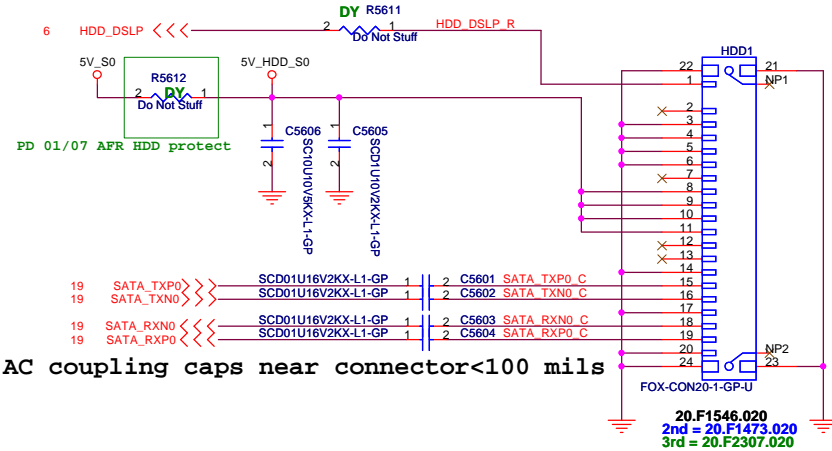
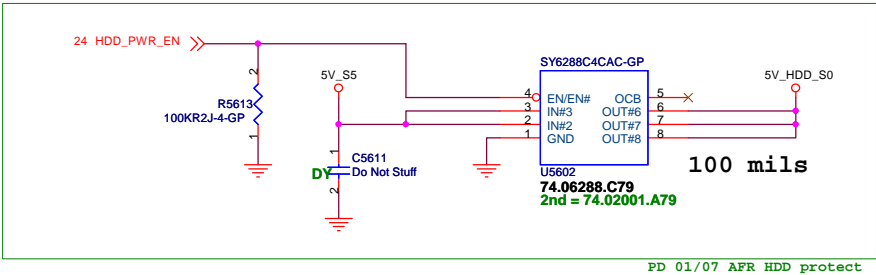


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Taipei Hsien 221, Taiwan, R.O.C.

HDMI Level Shifter/Connector			
Size	Project Name	KABINI	Rev SA
Date	Thursday, February 21, 2013	Sheet 54	of 102

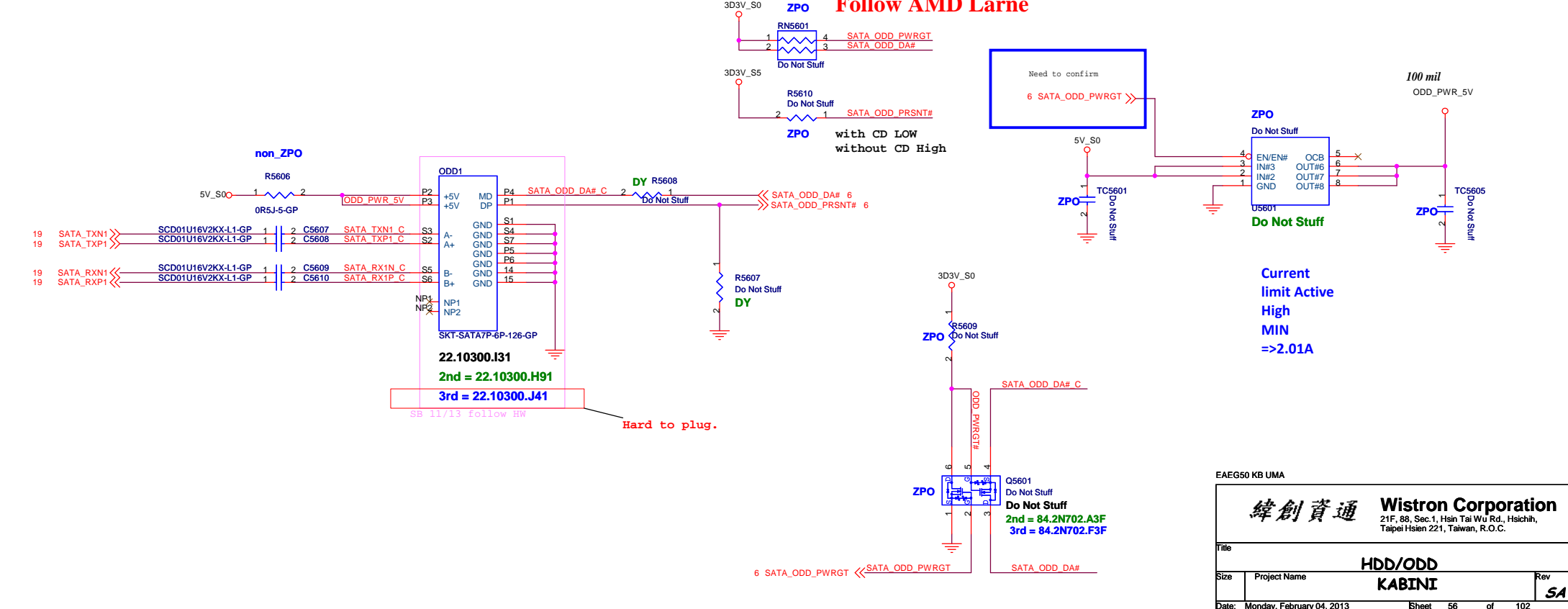
SSID = SATA

SATA HDD Connector



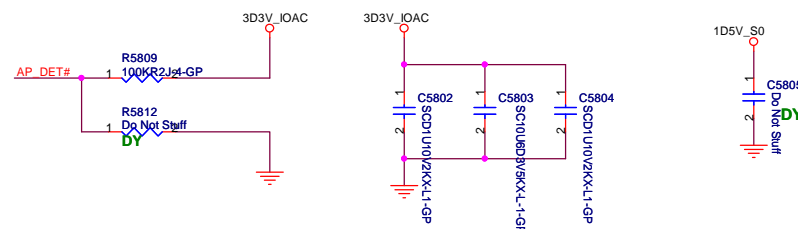
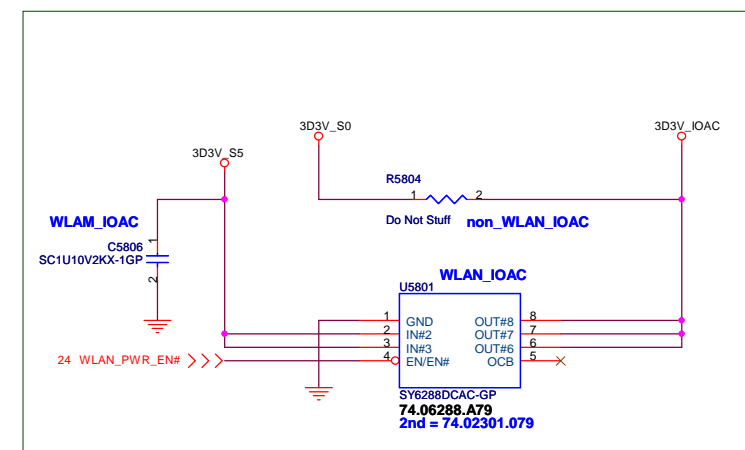
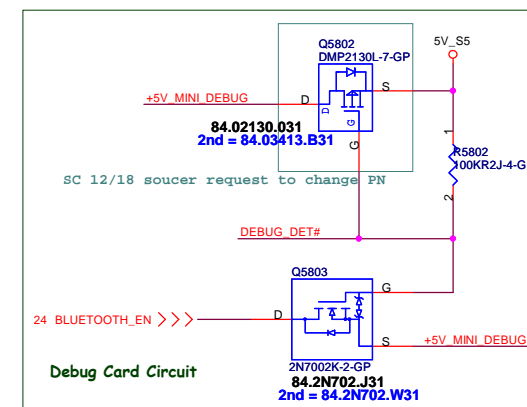
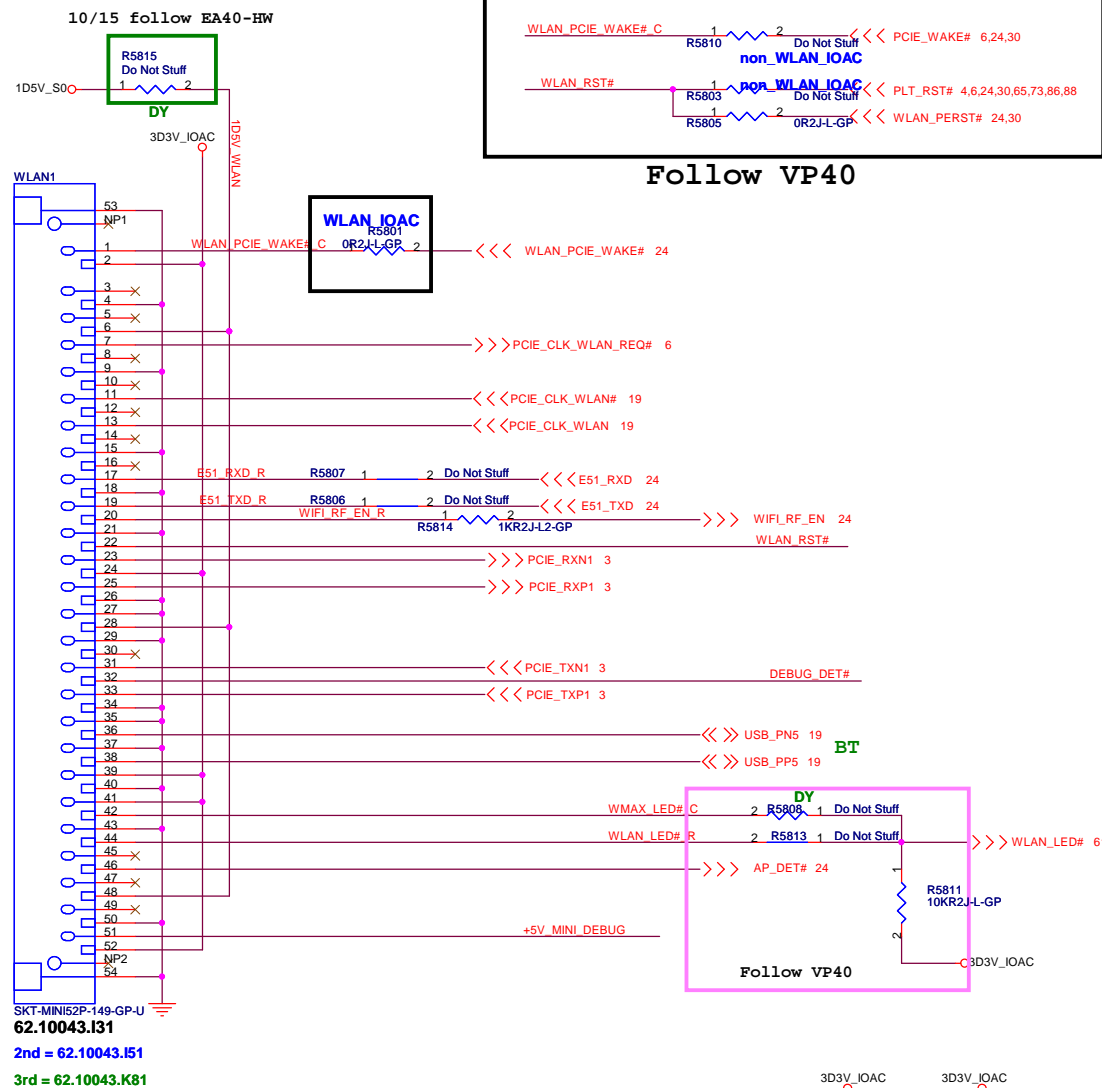
ODD Connector

SATA Zero Power ODD Follow AMD Larne



SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



SSID = Wireless

Mini Card Connector(WWAN)

EAEG50 KB UMA

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

WWAN CONN

Size

Project Name

KABINI

Rev

SA

Date: Friday, September 07, 2012

Sheet 59 of 102

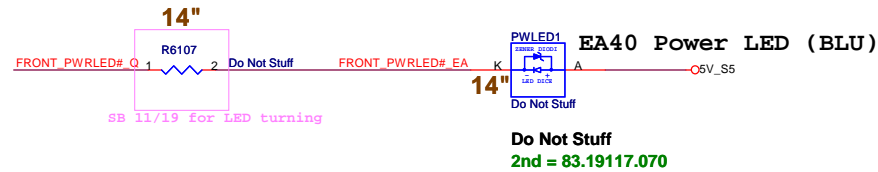
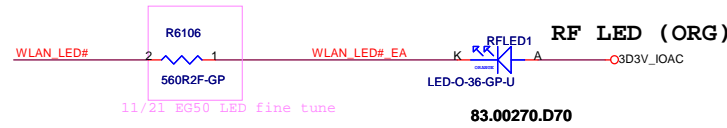
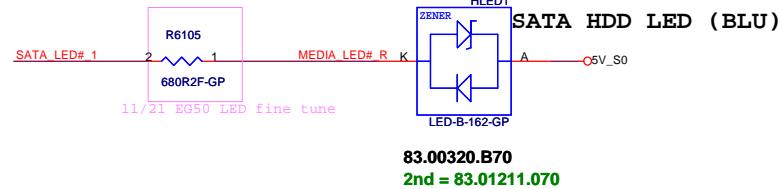
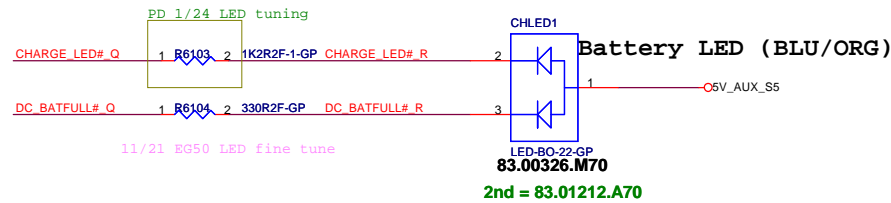
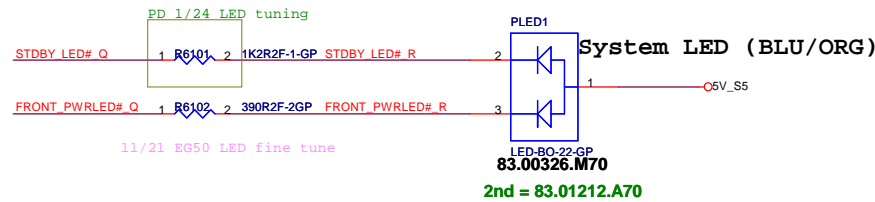
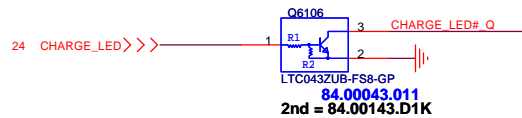
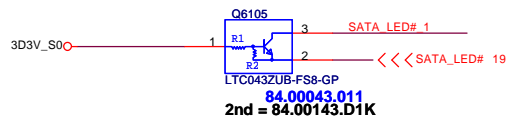
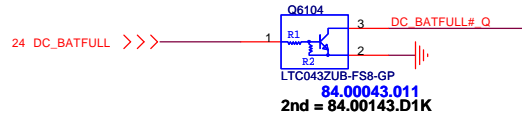
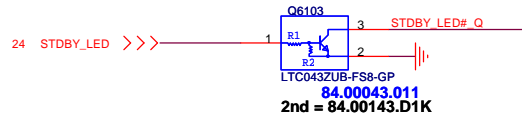
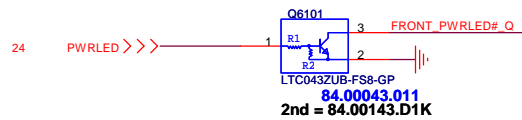
SSID = mSATA

Mini Card Connector(mSATA)

EAEG50 KB UMA

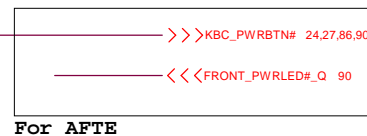
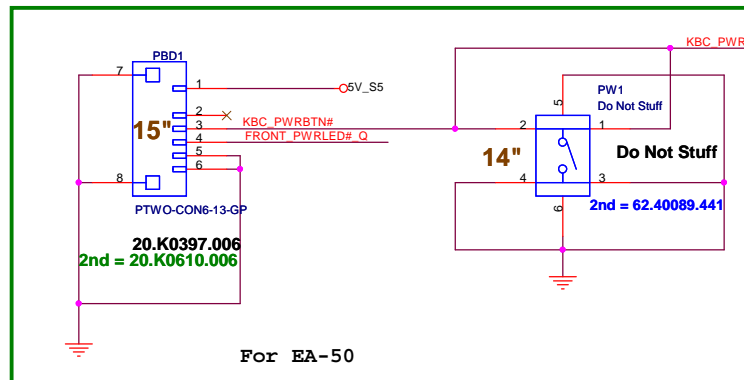
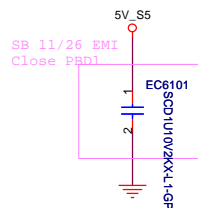
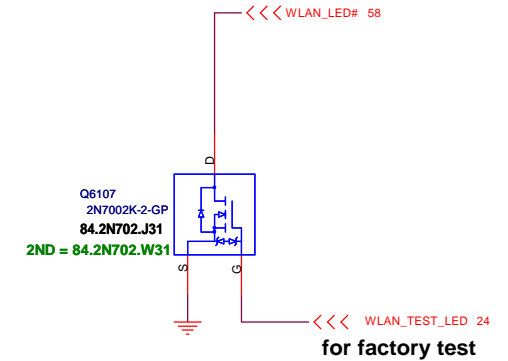
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title mSATA Connector		
Size	Project Name KABINI	Rev SA
Date: Friday, September 07, 2012		Sheet 60 of 102

SSID = User.Interface



WLAN_LED

From module



EAEG50 KB UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

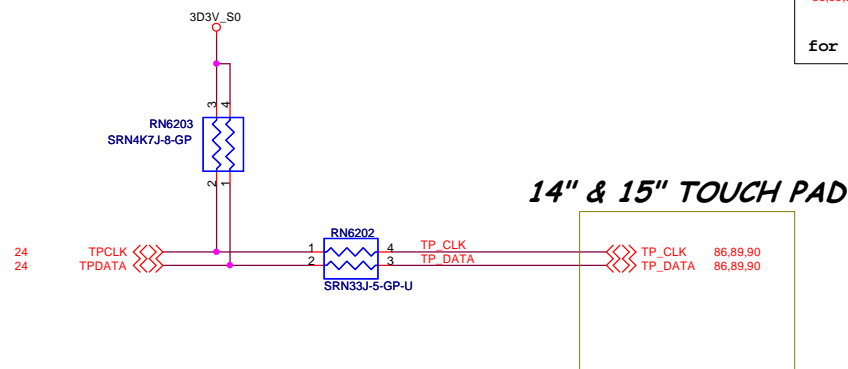
Title				
LED Bard/Power Button				
Size	Project Name			Rev
	KABINI			SA
Date:	Monday, February 04, 2013		Sheet 61 of 102	

SSID = KBC

Internal KeyBoard Connector

86,89,90 TP_DATA >>>
86,89,90 TP_CLK >>>
86,89,90 SWR >>>
86,89,90 SWL >>>

for AFTP



PD 1/14 Different 14" & 15" TOUCH PAD reversion

14"& 15" use the same KB

for EA/EG-50

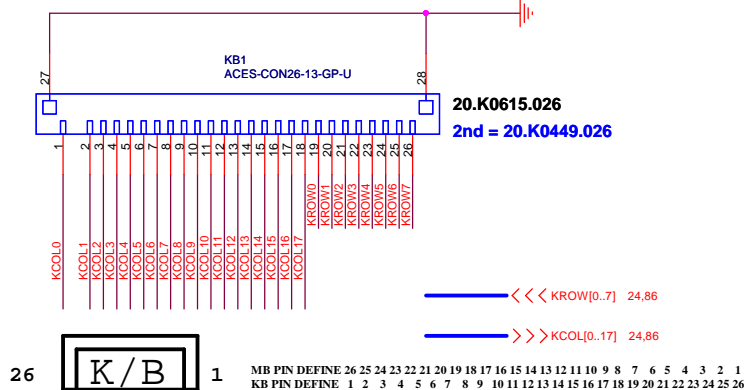
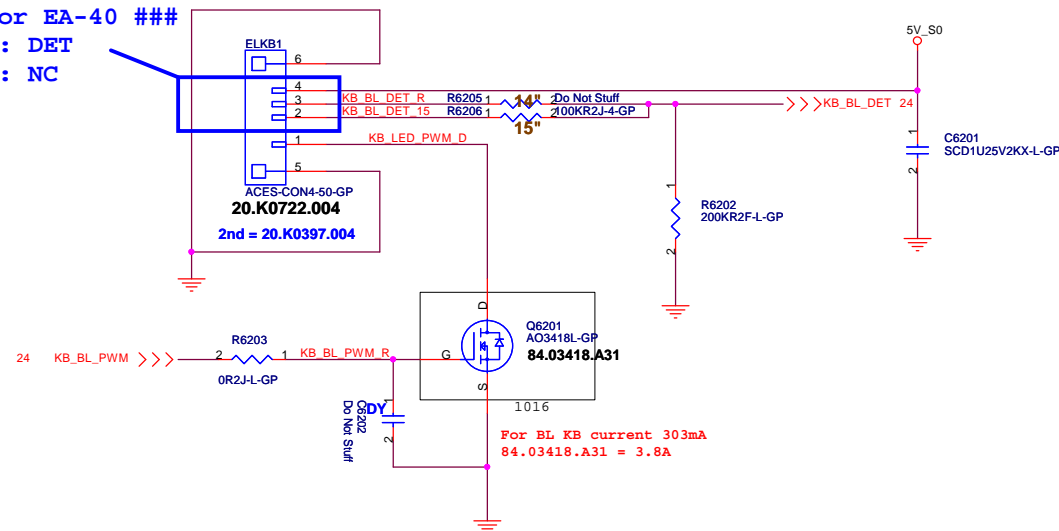
Pin3 : NC

Pin2 : DET

for EA-40

Pin3 : DET

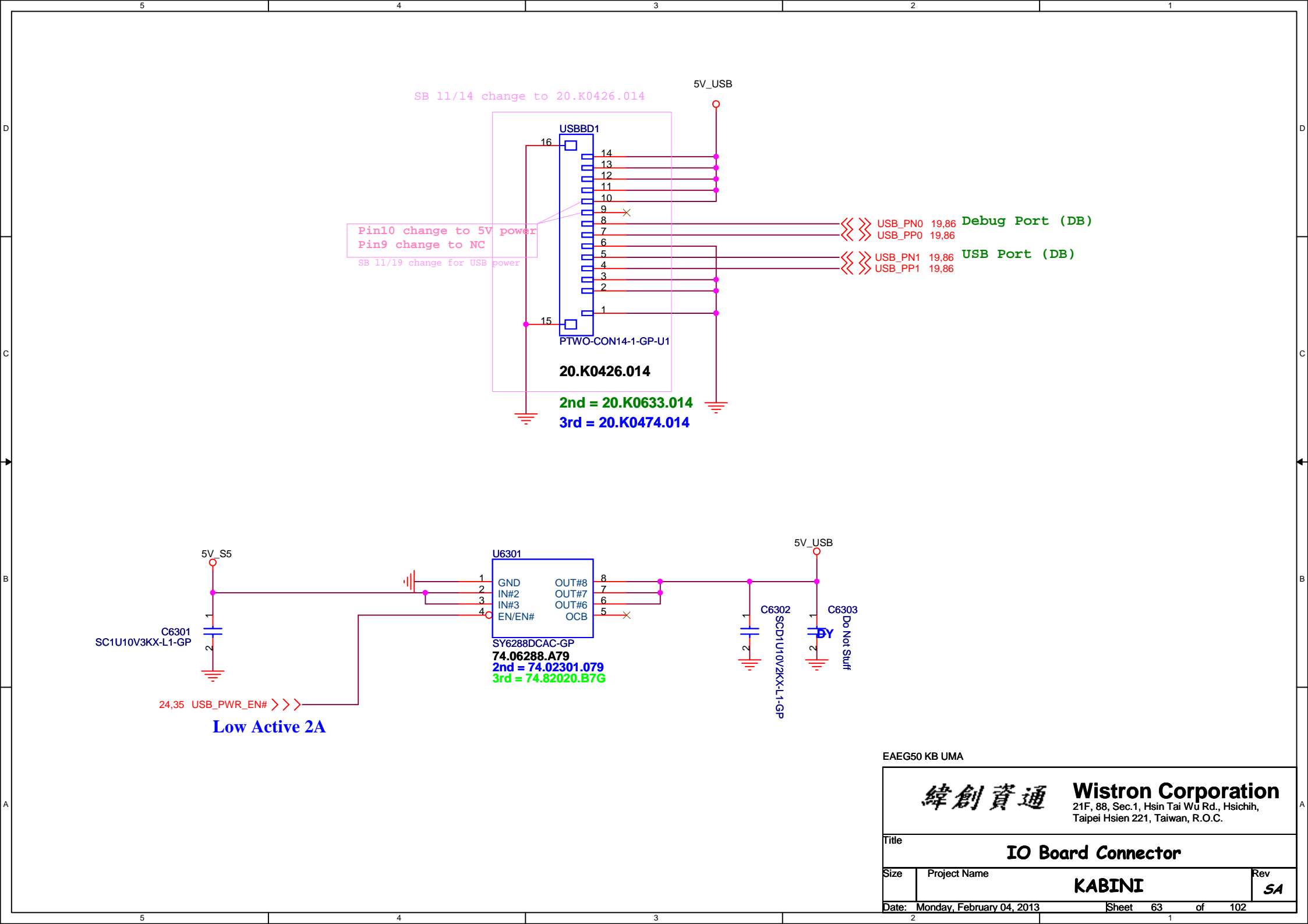
Pin2 : NC

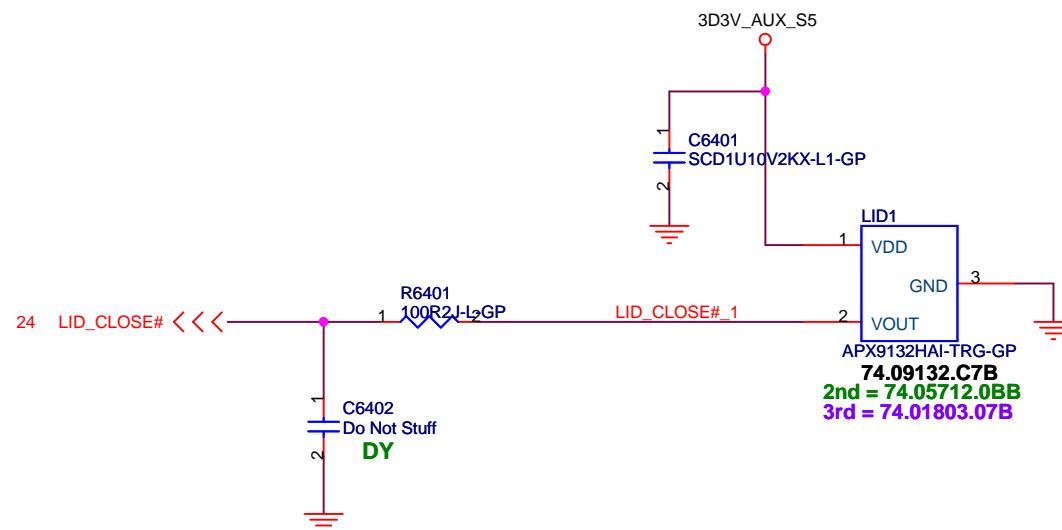


EAEG50 KB UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			Key Board/Touch Pad	
Size	Project Name	KABINI		Rev
				SA
Date:	Tuesday, February 19, 2013	Sheet	62	of 102





EAEG50 KB UMA

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Hall Sensor

Size

Project Name

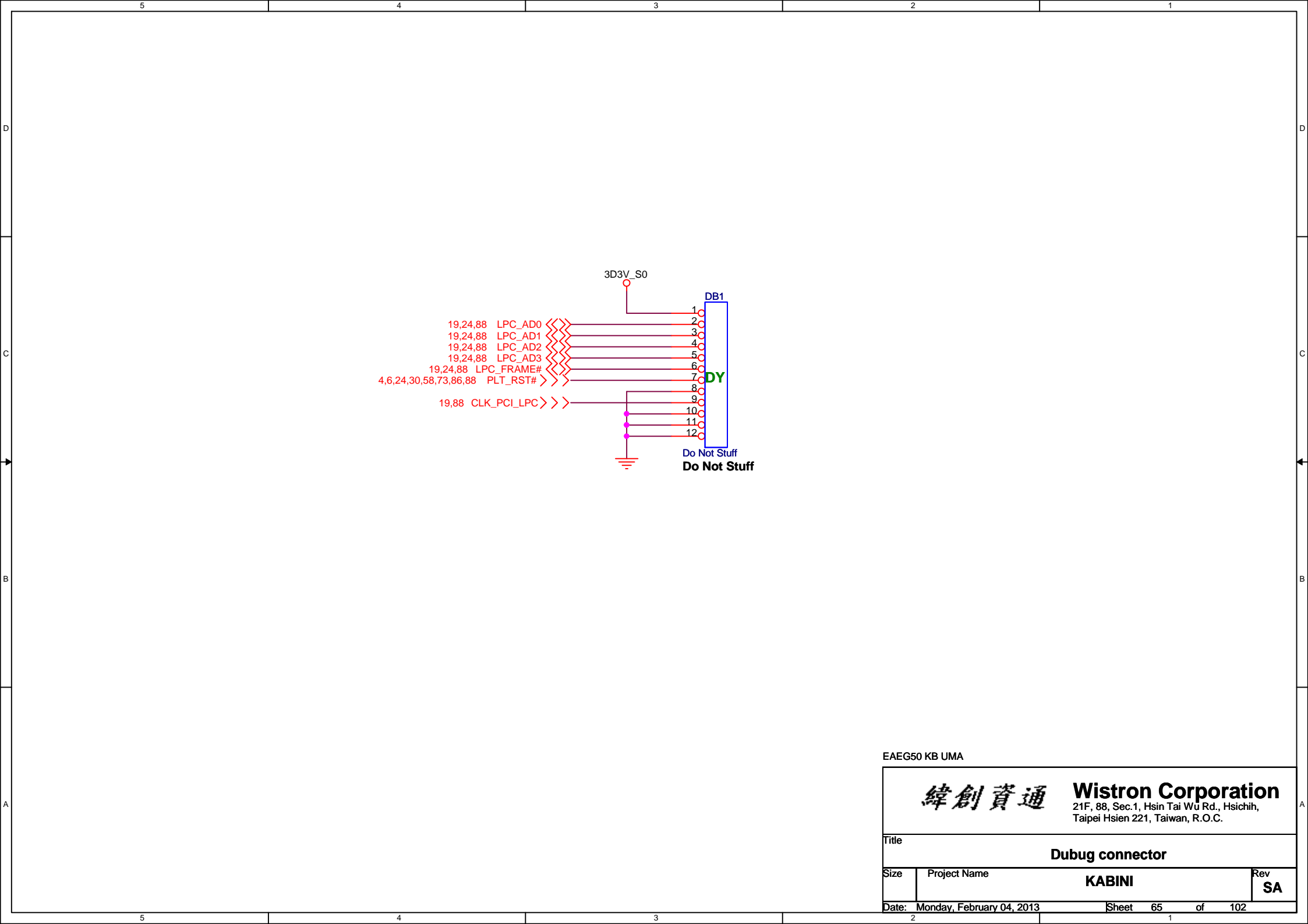
KABINI

Rev


SA

Date: Monday, February 04, 2013

Sheet 64 of 102



EAEG50 KB UMA

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Dubug connector			
Size	Project Name		Rev
	KABINI		SA
Date:	Monday, February 04, 2013	Sheet	65 of 102

(Blanking)

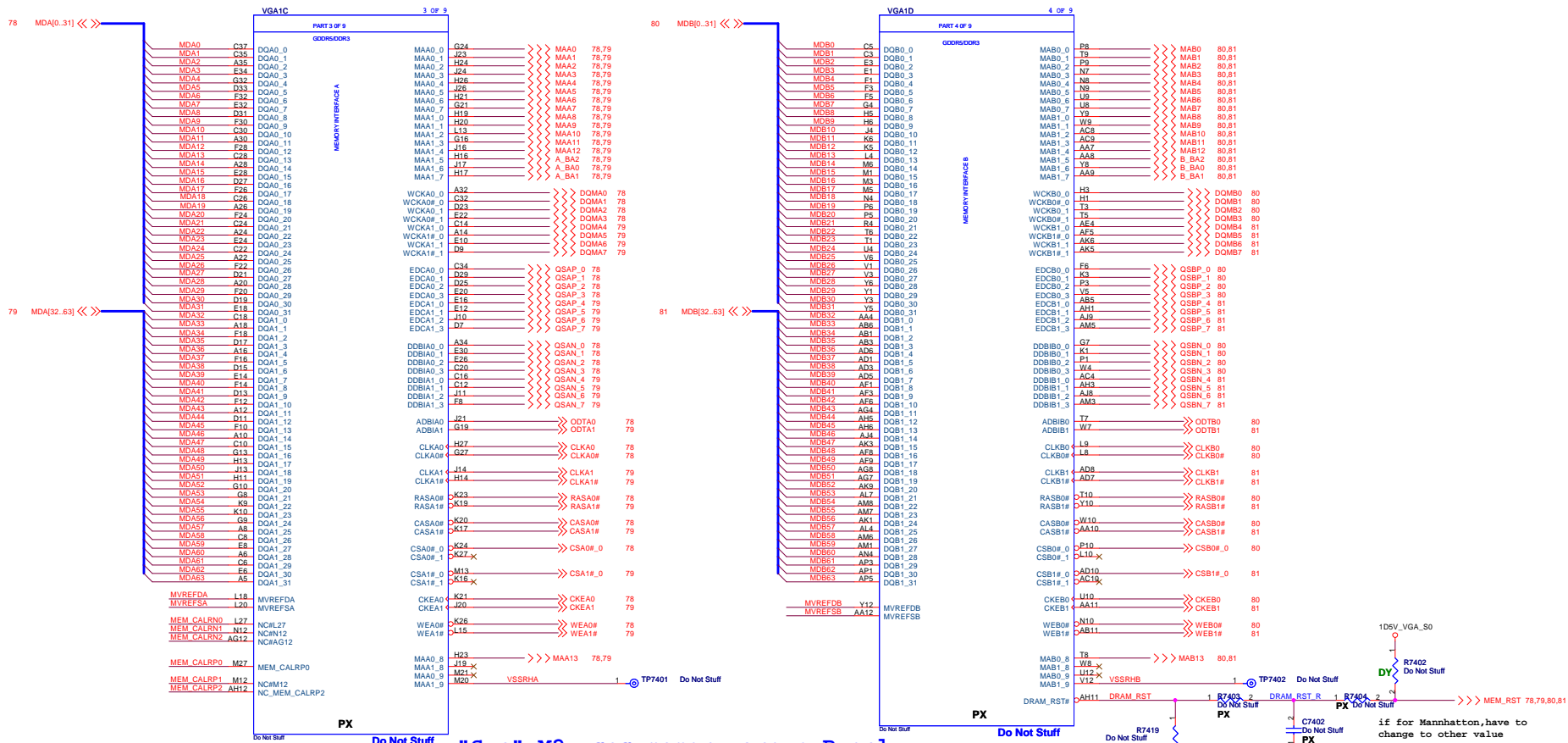
EAEG50 KB UMA

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title Reserved		
Size	Project Name KABINI	Rev SA
Date: Friday, September 07, 2012		Sheet 66 of 102

SSID = User.Interface

EAEG50 KB UMA

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
G Sensor			
Size	Project Name		Rev
	KABINI		SA
Date: Friday, September 07, 2012		Sheet	67 of 102



"Sun"-M2 uses memory group B only,
while "Sun"-S3 uses memory group A only

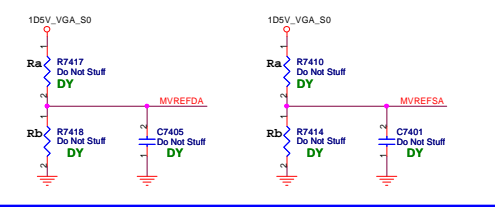
This basic topology should be used for DRAM_RAT for DDR3/GDDR5

PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

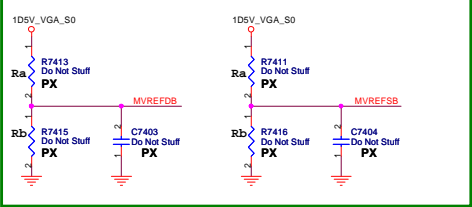
DDR3/GDDR3 Memory Stuff Option(Mad/Park)

	DDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

SUN S3 package



SUN M2 package

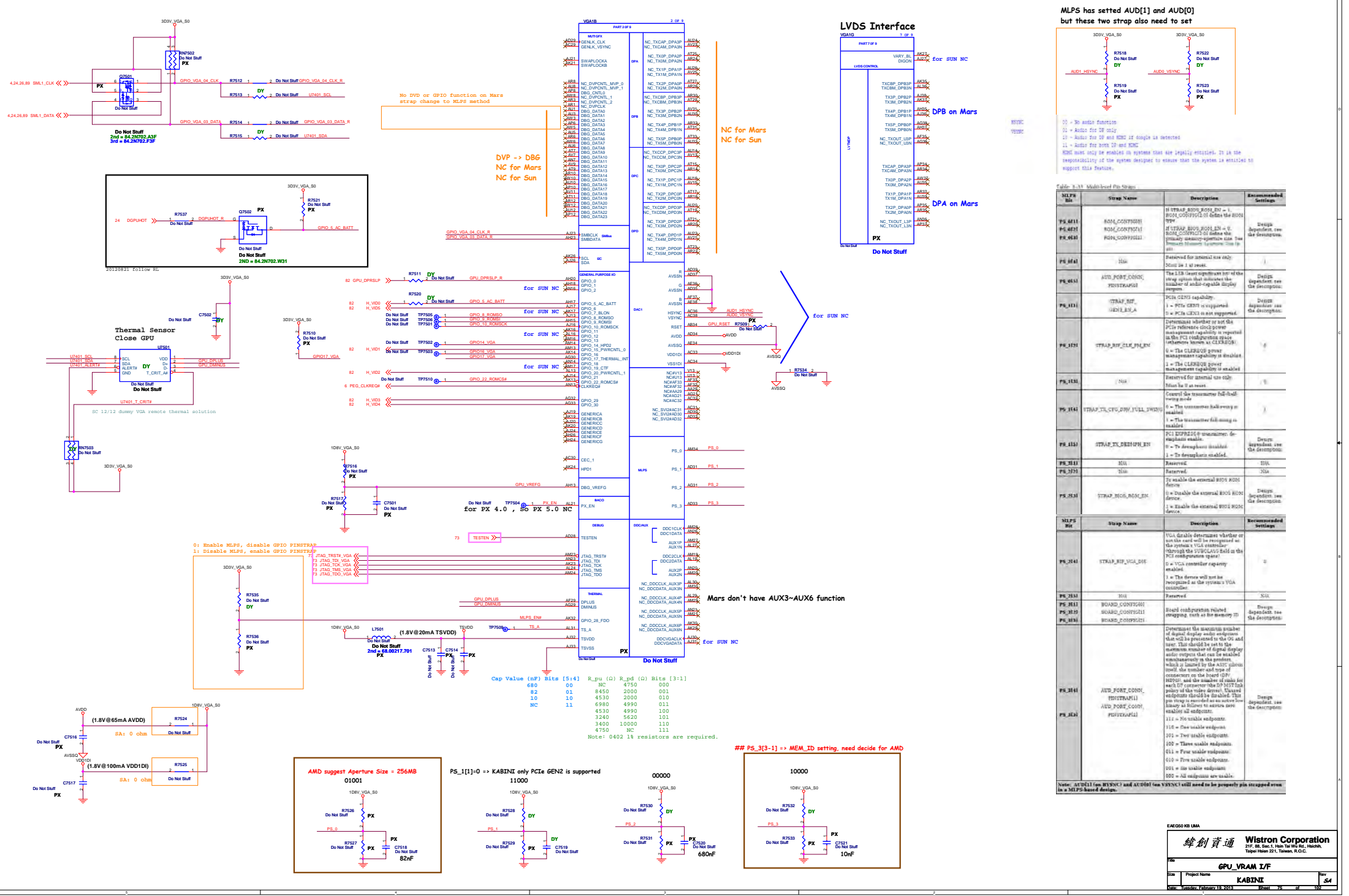


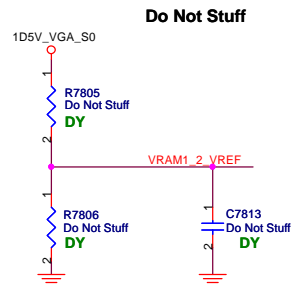
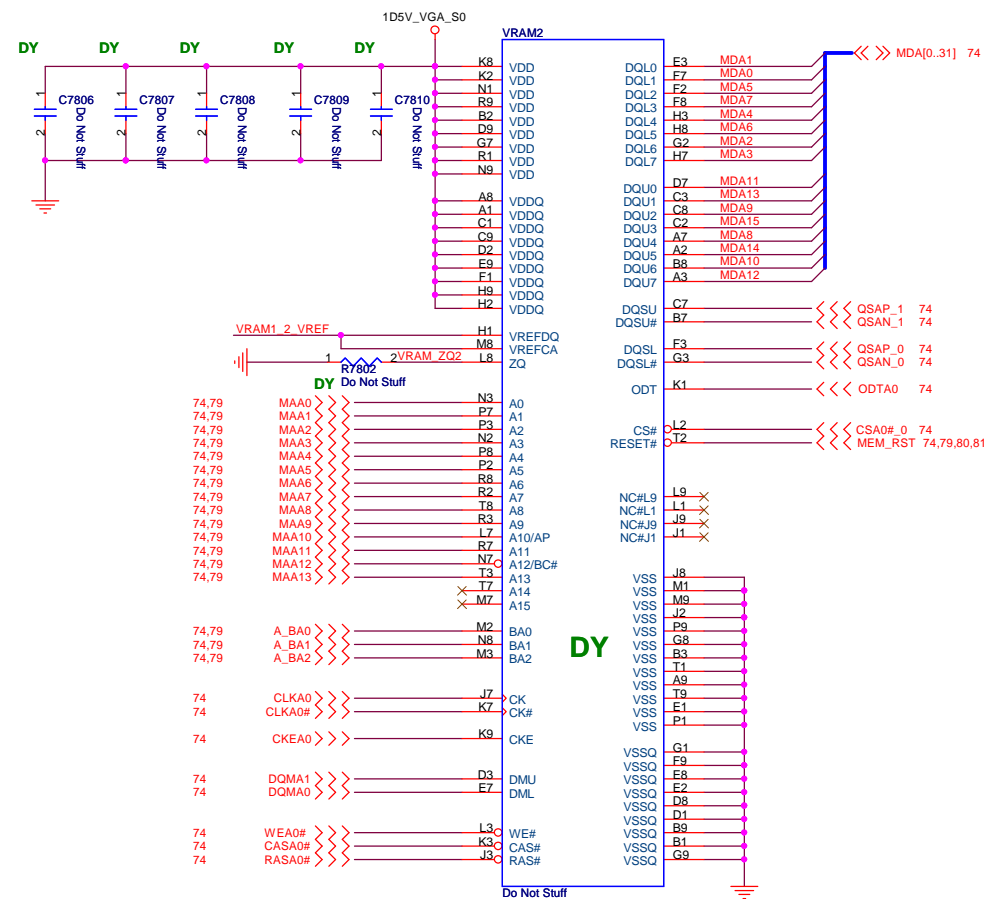
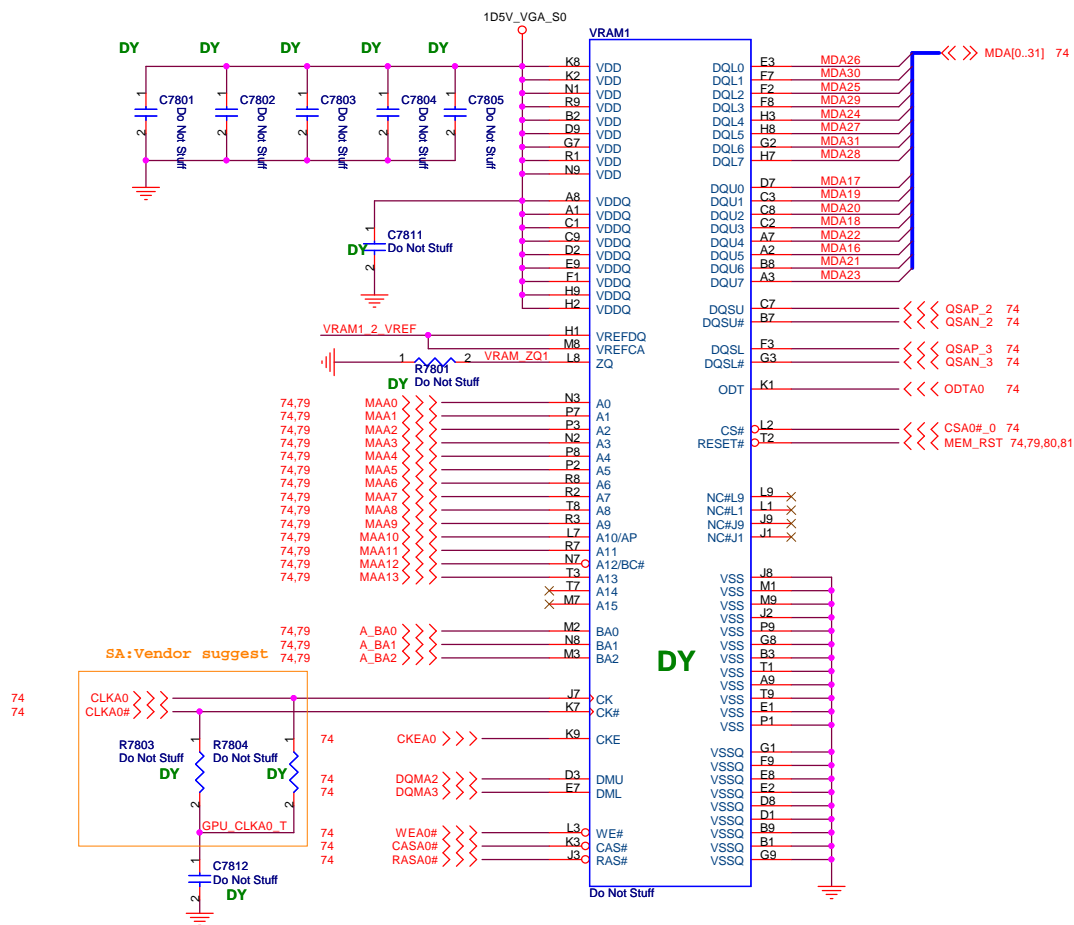
MEM_CALRN0	Whistler/Thames: Connect to VDDR1 through a 240Ω (40.5%) resistor. Prefered resistor tolerance is 0.5%, but 1% is acceptable. Seymour: NC Heathrow/Chelsea: NC	MEM_CALRP0	Whistler/Thames: need a 240Ω (1%) termination to ground. Seymour: NC Heathrow/Chelsea: Need a 120Ω (1%) termination to ground.
MEM_CALRN1	Whistler/Thames: NC Seymour: Connect to VDDR1 through a 240Ω (40.5%) resistor. Heathrow/Chelsea: NC	MEM_CALRP1	Whistler/Thames: NC Seymour: MEM_CALRP1—need a 240Ω (1%) termination to ground.
MEM_CALRN2	Whistler/Thames: Connect to VDDR1 through a 240Ω (40.5%) resistor. Seymour: NC Heathrow/Chelsea: NC	MEM_CALRP2	Whistler/Thames: MEM_CALRP2—need a 240Ω (1%) termination to ground. Seymour: NC Heathrow/Chelsea: Need a 120Ω (1%) termination to ground.

EAE50 KB UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.

File: **GPU_Digitalout**
Size: Project Name: **KABINI** Rev: **54**
Date: Monday, February 04, 2013 Sheet: 74 of 102



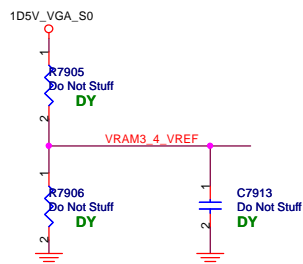
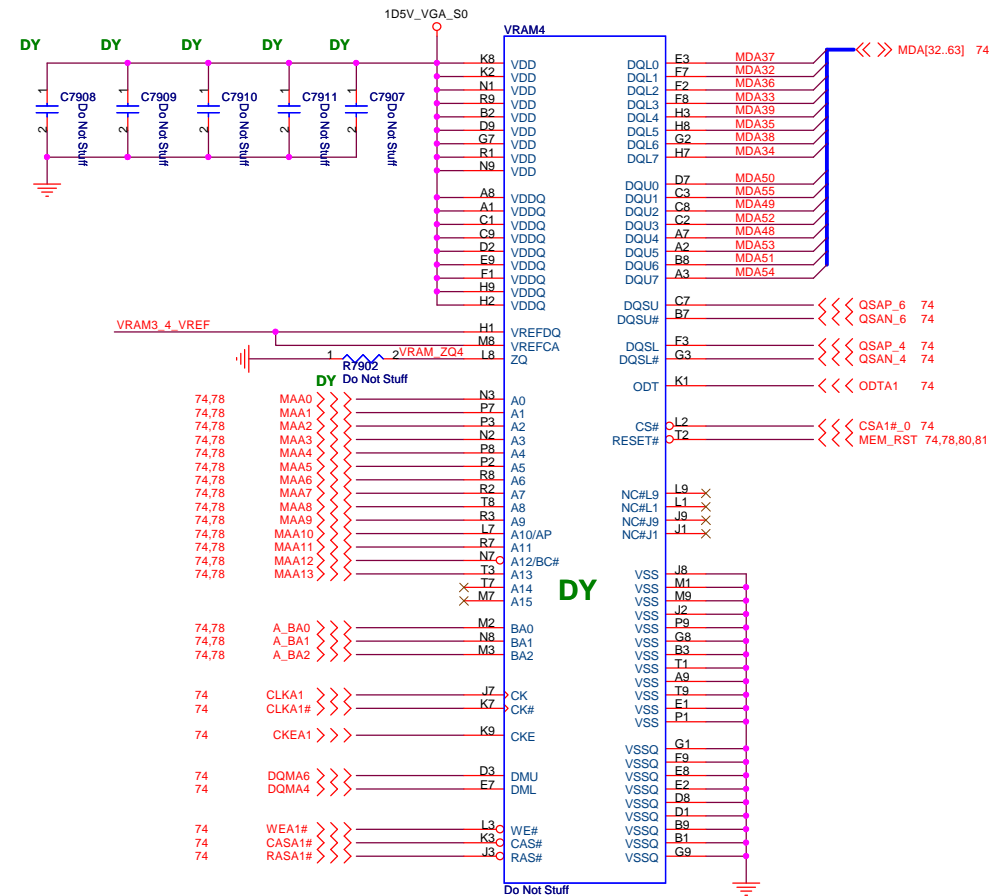
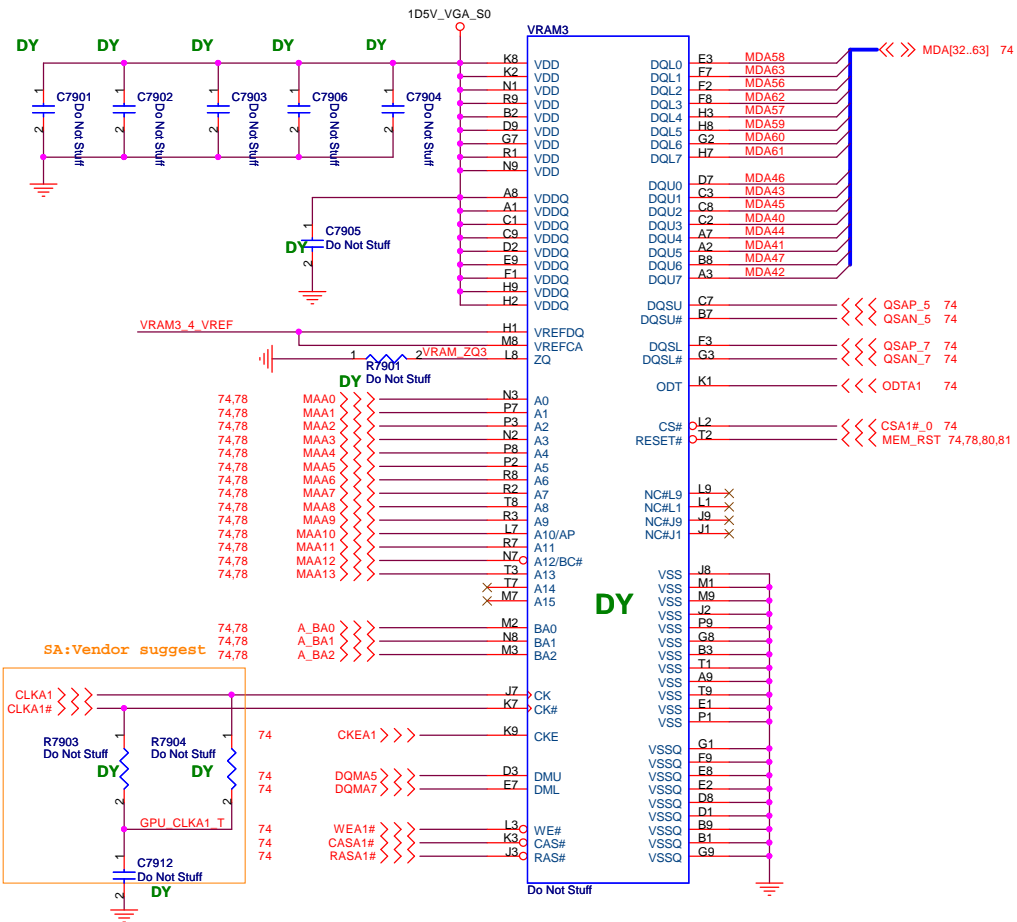


Do Not Stuff

EAEG50 KB UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title				
VRAM 1,2				
Size	Project Name			Rev
	KABINI			SA
Date:	Monday, February 04, 2013		Sheet 78 of 102	

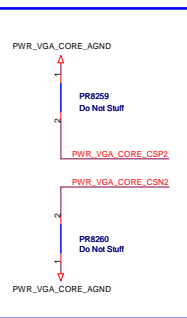
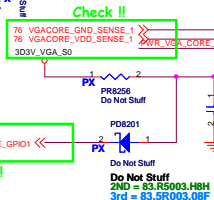
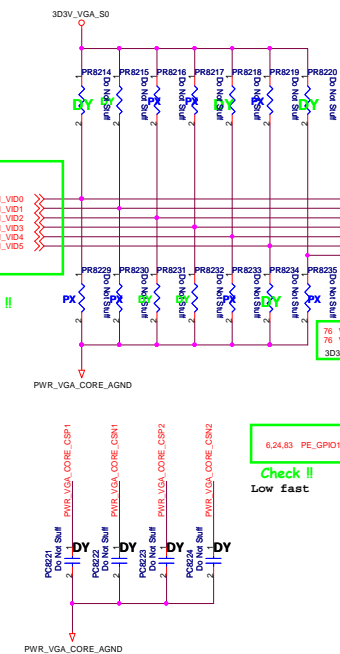
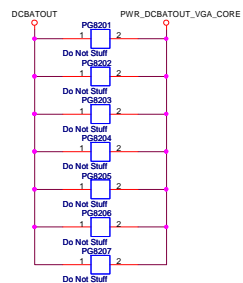


EAEG50 KB UMA

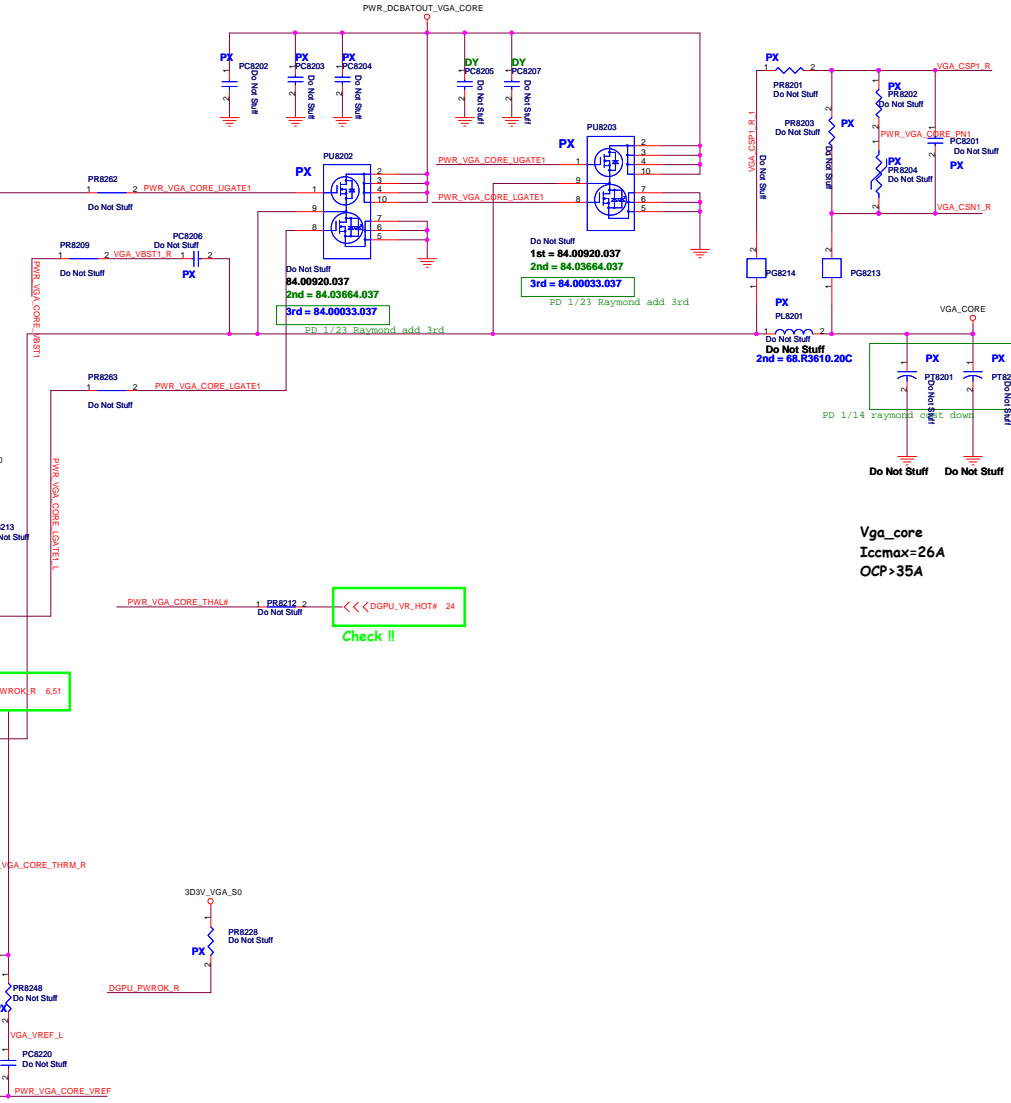
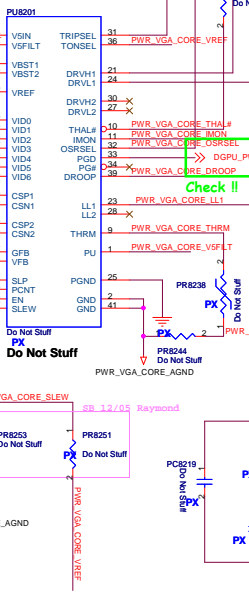
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsein 221, Taiwan, R.O.C.

Title			VRAM 3,4	
Size			KABINI	
Date: Monday, February 04, 2013			Rev 5A	
Sheet 79			of 102	


```
SSID = PWR.Plane.Regulator_GFX
```



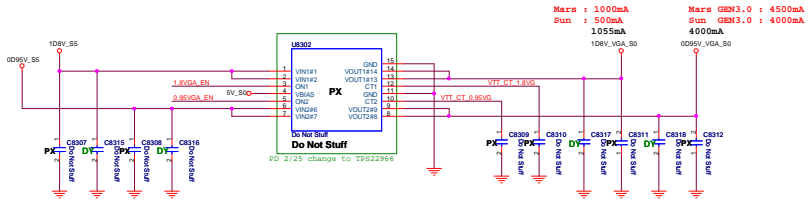
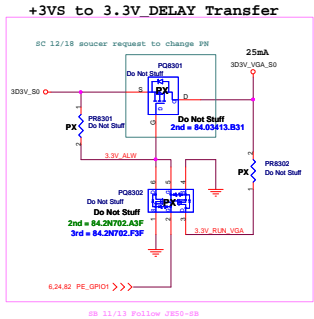
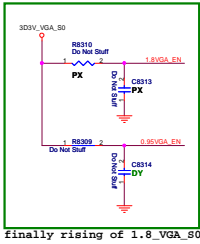
1phase PR8259 , PR8260 mount
2phase PR8259 , PR8260 DY



Vga_core
Iccmax=26A
OCP>35A

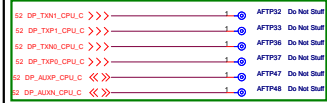
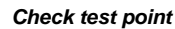
APL3523 for VGA_Power

	FE_GP100	FE_GP101
dGPU mode	H	H
IGPU	L	L
IGPU with BACO	H	H



EM6050 KB LMA

SB 11/14 follow HW for factory issue



EDP + MIC connector



LAN_RJ45 connector



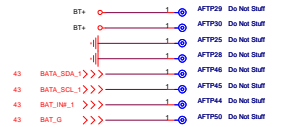
Card reader connector



USBBD connector



DC IN connector



Battery connector



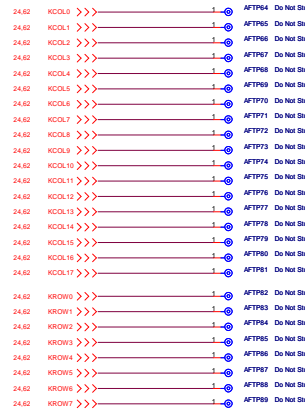
Speaker connector



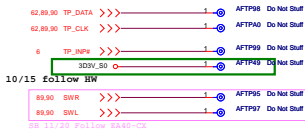
HP connector



FAN connector

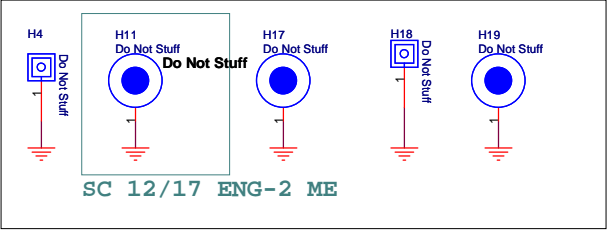


Normal KB connector

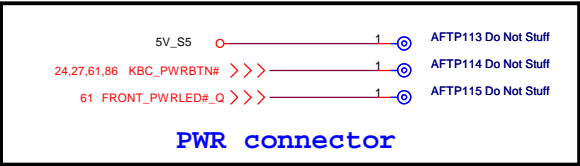


Touch Pad connector

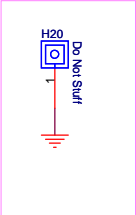
H4 & H11 & H17 & H18 & H19 for EG50



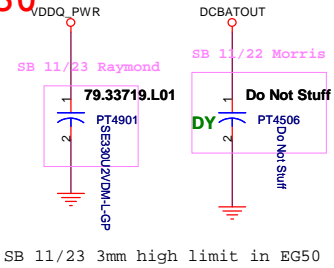
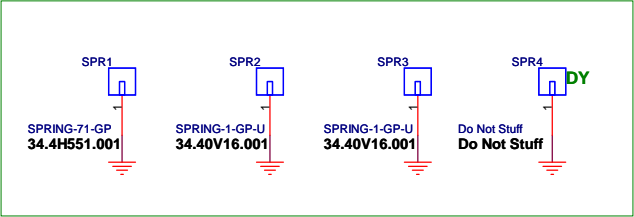
PWRBD AFTP for EG50



ZZ.00PAD.571

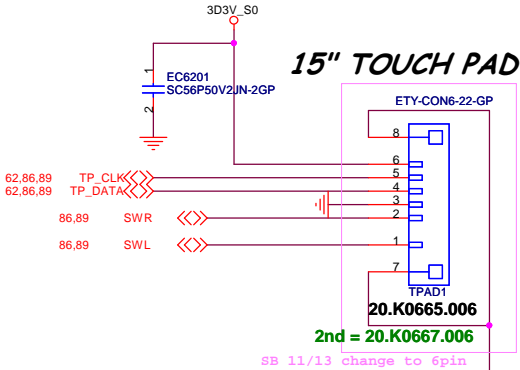
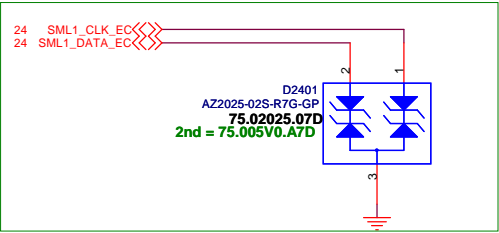


PD 1/23 EMI Jen



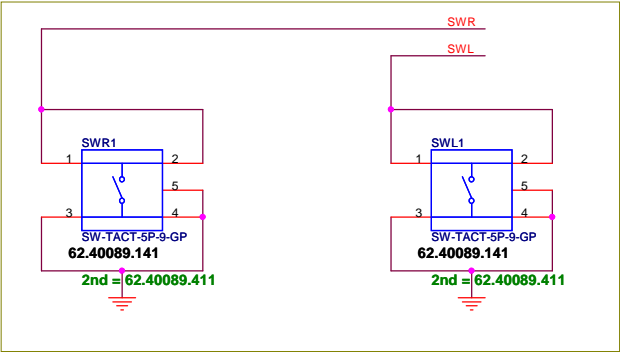
SB 11/23 3mm high limit in EG50

PD 01/31 Different Net name in 14" & 15" for placement



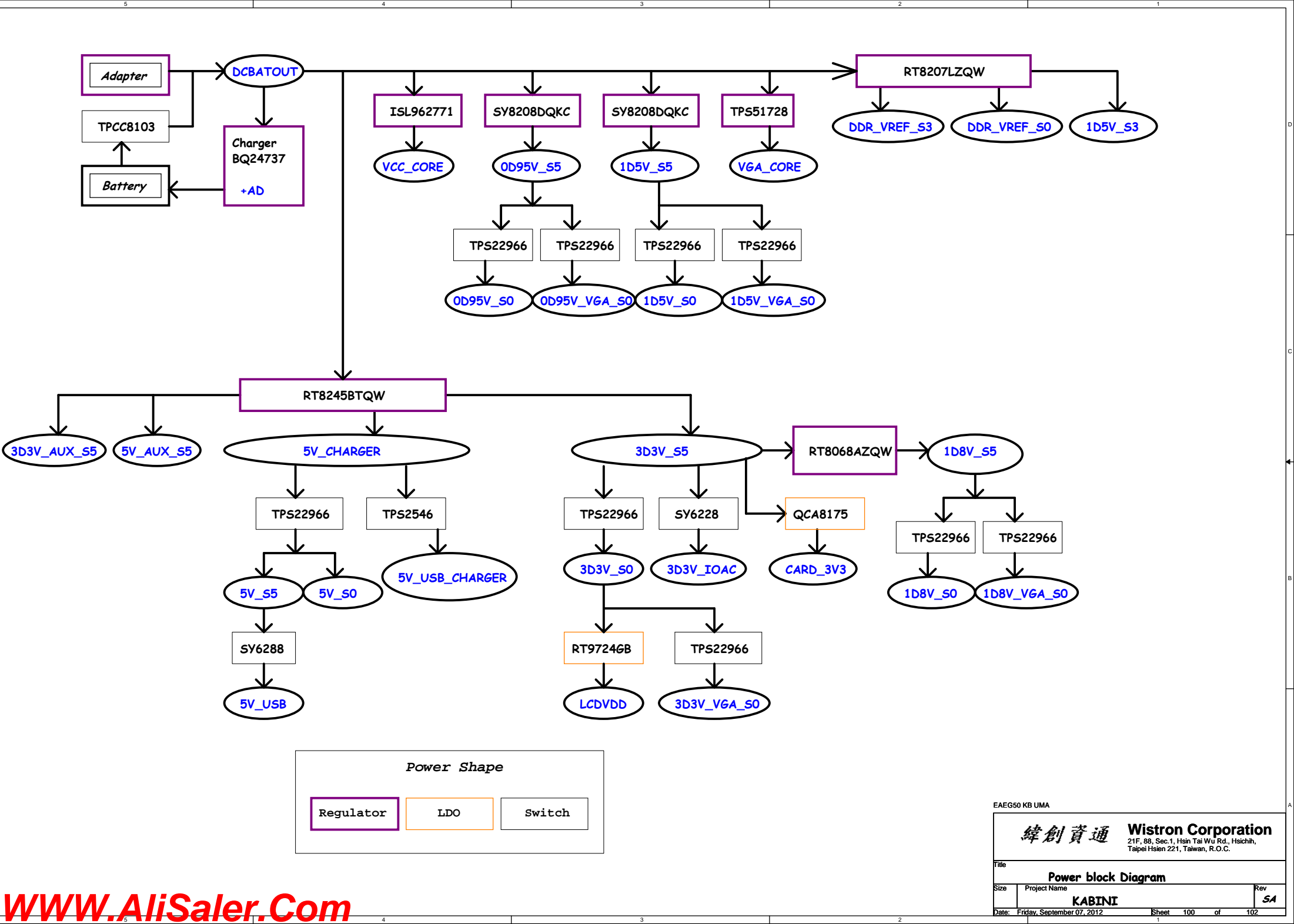
24,62,86	KCOL0	>>>
24,62,86	KCOL1	>>>
24,62,86	KCOL2	>>>
24,62,86	KCOL3	>>>
24,62,86	KCOL4	>>>
24,62,86	KCOL5	>>>
24,62,86	KCOL6	>>>
24,62,86	KCOL7	>>>
24,62,86	KCOL8	>>>
24,62,86	KCOL9	>>>
24,62,86	KCOL10	>>>
24,62,86	KCOL11	>>>
24,62,86	KCOL12	>>>
24,62,86	KCOL13	>>>
24,62,86	KCOL14	>>>
24,62,86	KCOL15	>>>
24,62,86	KCOL16	>>>
24,62,86	KCOL17	>>>
24,62,86	KROW0	>>>
24,62,86	KROW1	>>>
24,62,86	KROW2	>>>
24,62,86	KROW3	>>>
24,62,86	KROW4	>>>
24,62,86	KROW5	>>>
24,62,86	KROW6	>>>
24,62,86	KROW7	>>>

For AFTE

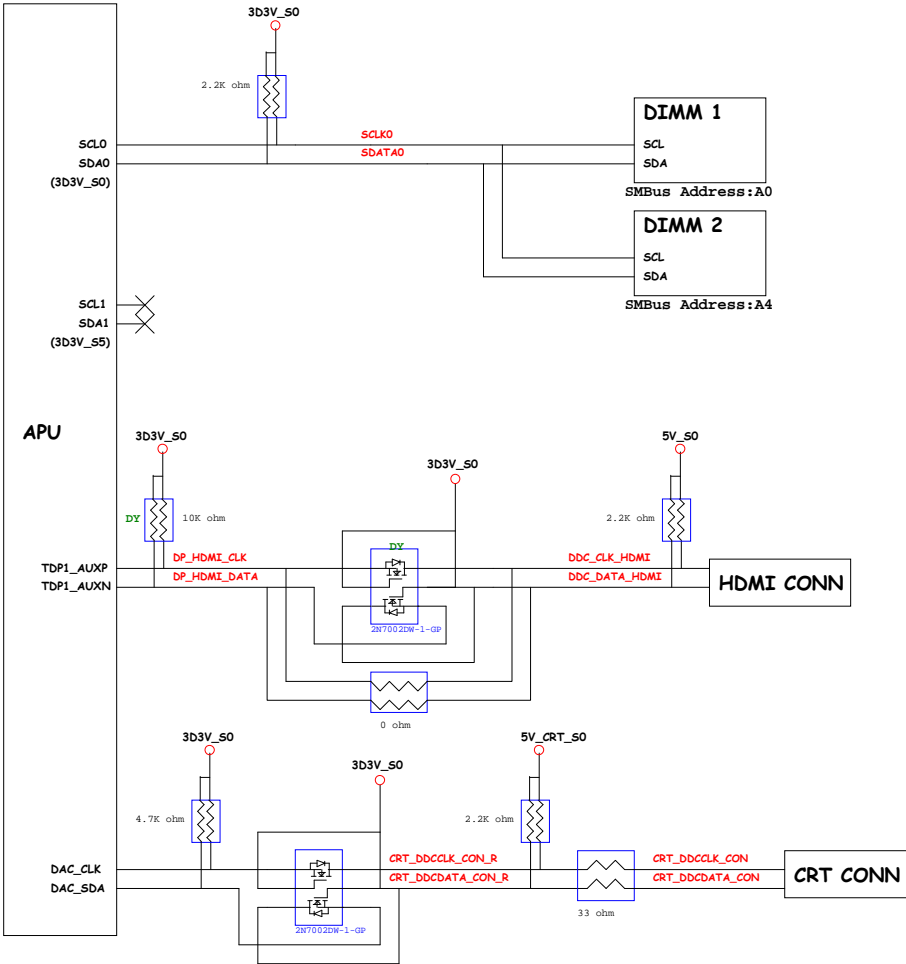


PD 1/21
SWL1 / SWR1 1st change to 62.40089.141, 2nd change to 62.40089.411 ,
because 160kg change to 100kg.

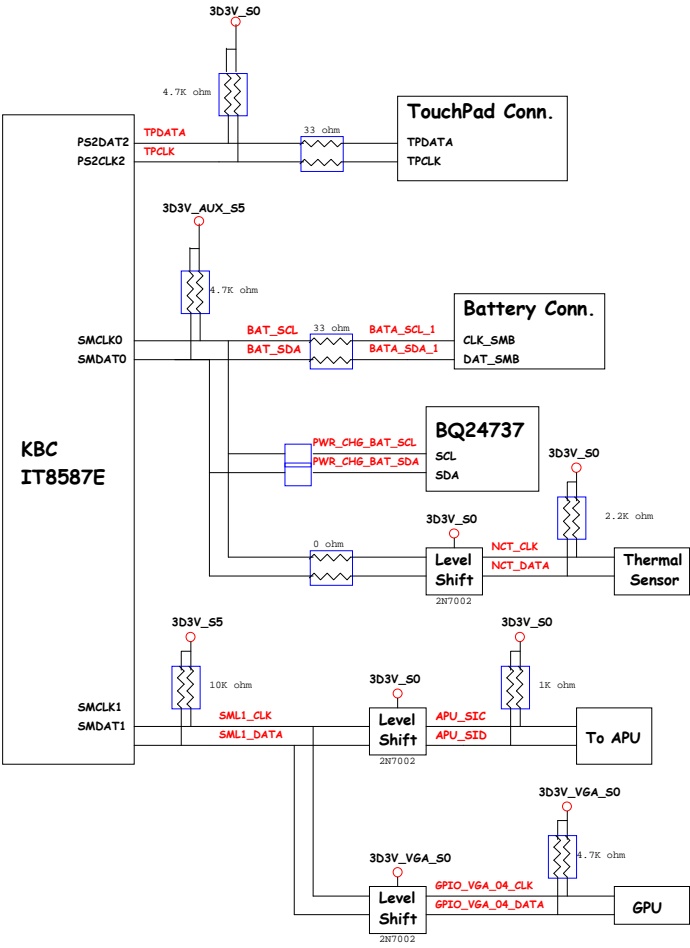
EAEG50 KB UMA



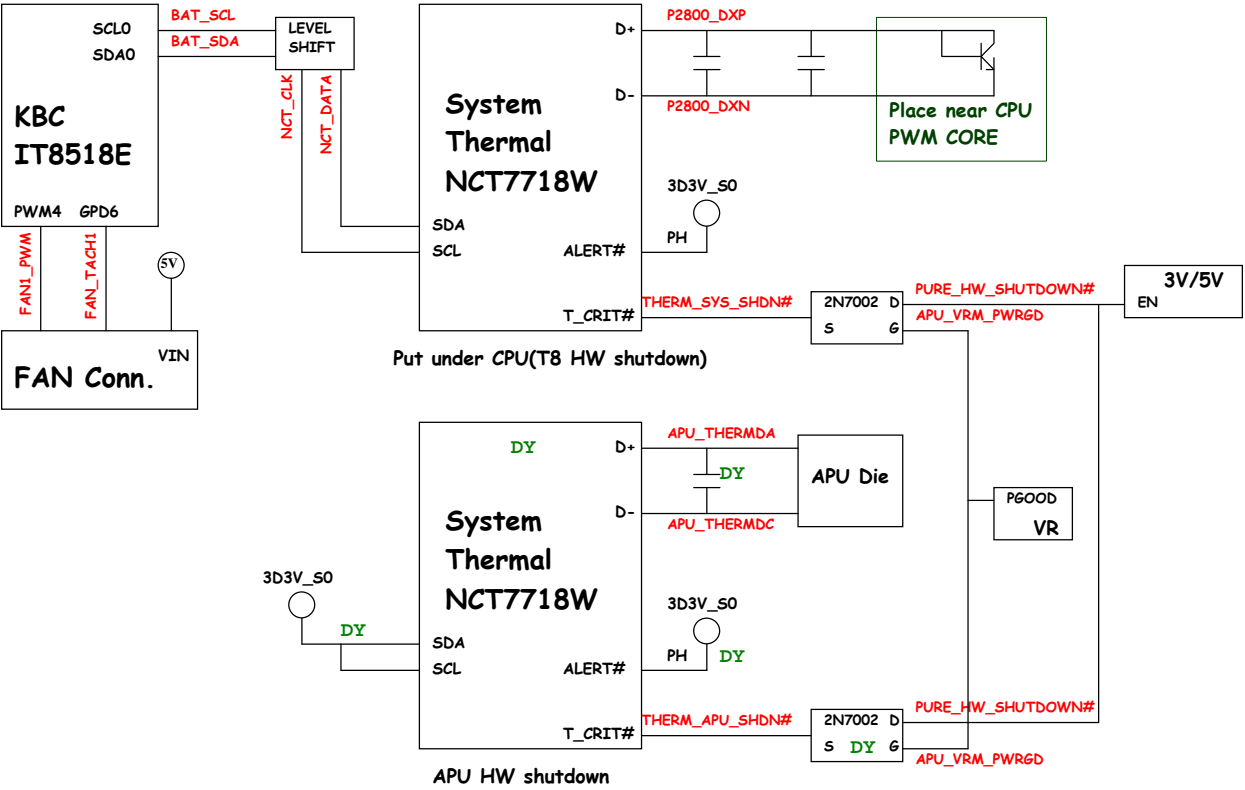
SMBus Block Diagram



KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram

